F71869A

Super I/O + Hardware Monitor

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F71869A Datasheet Revision History

Version	Date	Page	Revision History
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0.11P	2010/05	45, 46 47-136	1. Update CIR/CPT function description 2. Update Register
0.12P	2010/06	19 47, 48 65, 66 142-144 10-20 70 90, 91 60, 61 10 140 13, 21 56 74 129, 130 132 133 148	1. Modify pin54 description 2. Add scan code and OVT function description 3. Update RS485 enable register description — Index F0h 4. DC Characteristics 5. Update Pin Description 6. Update OVT register — Index 02h 7. Update Fan3 control register — Index 9Ah 8. Add Multi-Function Select Register 5 — Index 2Ch 9. Correct Pin Type 10. Add Intel DSW Delay Select Register— Index FCh 11. Update STRAP_PROTECT description 12. Update Configuration Port Select Register — Index 27h 13. Add Voltage Protection Power Good Select Register — Index 3Fh 14. Add CIR Registers (CR08) 15. Update ERP PSOUT deb-register — Index E5h; ERP S5 Delay Register — Index E7h 16. Update ERP WDT Timer — Index EEh 17. Update Application Circuit — S5# (S4#) , SUS_ACK# (3VA)
0.13P	2010/07	147	1. Update Application Circuit – Correct VIN5 pin name

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1. General Description

The F71869A which is the featured IO chip for PC system is equipped with one IEEE 1284 Parallel Port, two UART Ports, one 80 port (multi with COM2), Hardware Keyboard Controller, SIR, CIR with RC6 and SMK QP protocols and one FDC. The F71869A integrates with hardware monitor, 9 sets of voltage sensor, 3 sets of creative auto-controlling fans and 3 temperature sensor pins for the accurate dual current type temperature measurement for CPU thermal diode or external transistors 2N3906. Others, the F71869A supports newest AMD TSI and Intel PECI 3.0 interfaces and INTEL Ibex PEAK SMBus for temperature sensing and provides the power sequence controller function for AMD platform.

The F71869A provides flexible features for multi-directional application. For instance, the F71869A provides 58 GPIO pins (multi-pin), IRQ sharing function also designed in UART feature for particular usage and accurate current mode H/W monitor will be worth in measurement of temperature, provides 3 modes fan speed control mechanism included Manual Mode/Stage Auto Mode/Linear Auto Mode for users' selection.

A power saving function which is in order to save the current consumption when the system is in the soft off state is also integrated a power saving function. The power saving function supports that system boot-on not only by pressing the power button but also by the wake-up event. When the system enters the S4/S5 state, F71869A can cut off the VSB power rail which supplies power source to the devices like the LAN chip, the chipset, the SIO, the audio codec, DRAM, and etc. The PC system can be simulated to G3-like state when system enters the S4/S5 states. At the G3-like state, the F71869A consumes the 5VSB power rail only. The integrated two control pins are utilized to turn on or off VSB power rail in the G3-like status. The turned on VSB rail is supplied to a wake up device to fulfill a low power consumption system which supports a wake up function.

These features as above description will help you more and improve product value. Finally, the F71869A is powered by 3.3V voltage, with the LPC interface in the green package of 128-LQFP (14*14).

2. Feature List

◆ **General Functions**

- ➢Comply with LPC Spec. 1.0
- ➢Support DPM (Device Power Management), ACPI
- ➢Support AMD power sequence controller
- ➢Provides one FDC, two UARTs, Hardware KBC and Parallel Port
- ➢H/W monitor functions
- ➢Support AMD TSI Interface, Intel PECI 3.0 interface, Intel Block Read/Write SMBus Interface
- ➢Support CIR with RC6 and SMK QP protocols
- ➢Support Intel Cougar Point Timing
- ➢58 GPIO Pins for flexible application
- ➢24/48 MHz clock input
- ➢Packaged in 128-LQFP and powered by 3.3VCC

◆ **FDC**

- ➢Compatible with IBM PC AT disk drive systems
- ➢Variable write pre-compensation with track selectable capability
- ➢Support vertical recording format
- ➢DMA enable logic
- ➢16-byte data FIFOs
- ➢Support floppy disk drives and tape drives
- ➢Detects all overrun and under run conditions
- ➢Built-in address mark detection circuit to simplify the read electronics
- ➢Completely compatible with industry standard 82077
- ➢360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate

◆ **UART**

- ➢Two high-speed 16C550 compatible UART with 16-byte FIFOs
- ➢Fully programmable serial-interface characteristics
- ➢Baud rate up to 115.2K
- ➢Support IRQ sharing
- ➢Support Ring-In Wakeup

◆ **Infrared**

- ➢Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps

◆ **Parallel Port**

- ➢One PS/2 compatible bi-directional parallel port
- ➢Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- ➢Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- ➢Enhanced printer port back-drive current protection

◆ **Keyboard Controller**

- ➢LPC interface support serial interrupt channel 1, 12.
- ➢Two 16bit Programmable Address fully decoder, default 0x60 and 0x64.
- ➢Support two PS/2 interface, one for PS/2 mouse and the other for keyboard.
- ➢Keyboard's scan code support set1, set2.
- ➢Programmable compatibility with the 8042.
- ➢Support both interrupt and polling modes.
- ➢Fast Gate A20 and Hardware Keyboard Reset.

◆ **Hardware Monitor Functions**

- ➢3 dual current type (±3℃) thermal inputs for CPU thermal diode and 2N3906 transistors
- ➢Temperature range -40℃~127℃
- ➢9 sets voltage monitoring (6 external and 3 internal powers)
- ➢Voltage monitor supports Over Voltage Protection (OVP)
- ➢High limit signal (PME#) for Vcore level
- ➢3 fan speed monitoring inputs
- ➢3 fan speed PWM/DC control outputs(support 3 wire and 4 wire fans)
- ➢The Fan PWM output frequency can be programmed to 23.5K or 220Hz for LCD backlight adjustment
- ➢Stage auto mode (2-Limit and 3-Stage)/Linear auto mode/Manual mode
- ➢Issue PME# and OVT# hardware signals output
- ➢Case intrusion detection circuit
- ➢WATCHDOG comparison of all monitored values

◆ **Power Saving Controller**

- ➢ACPI Timing and Power Control
- ➢Wake-up Supported

◆ **Integrate AMD TSI Interface**

◆ **Integrate Intel PECI 3.0 Spec.**

◆ **Integrate Intel Cougar Point Timing**

◆ **Support AMD Power Sequence Controller**

◆ **Intel Block Read/Write SMBus Interface**

◆ **System volume control**

- GPIO 50 to GPIO 54 can control the system volume up/down/mute by LPC interface.
- Windows OSD can detect the system volume control input without any driver installation.

◆ **80-Port Interface**

- Monitor 0x80 Port and output the value via signals defined for 7-segment display.
- High nibble and low nibble are outputted interleaved at 1KHz frequency.
- 80-Port output by LPT or COM2 interface.

◆ **Package**

- 128-pin LQFP (14*14) Green Package

3. Pin Configuration

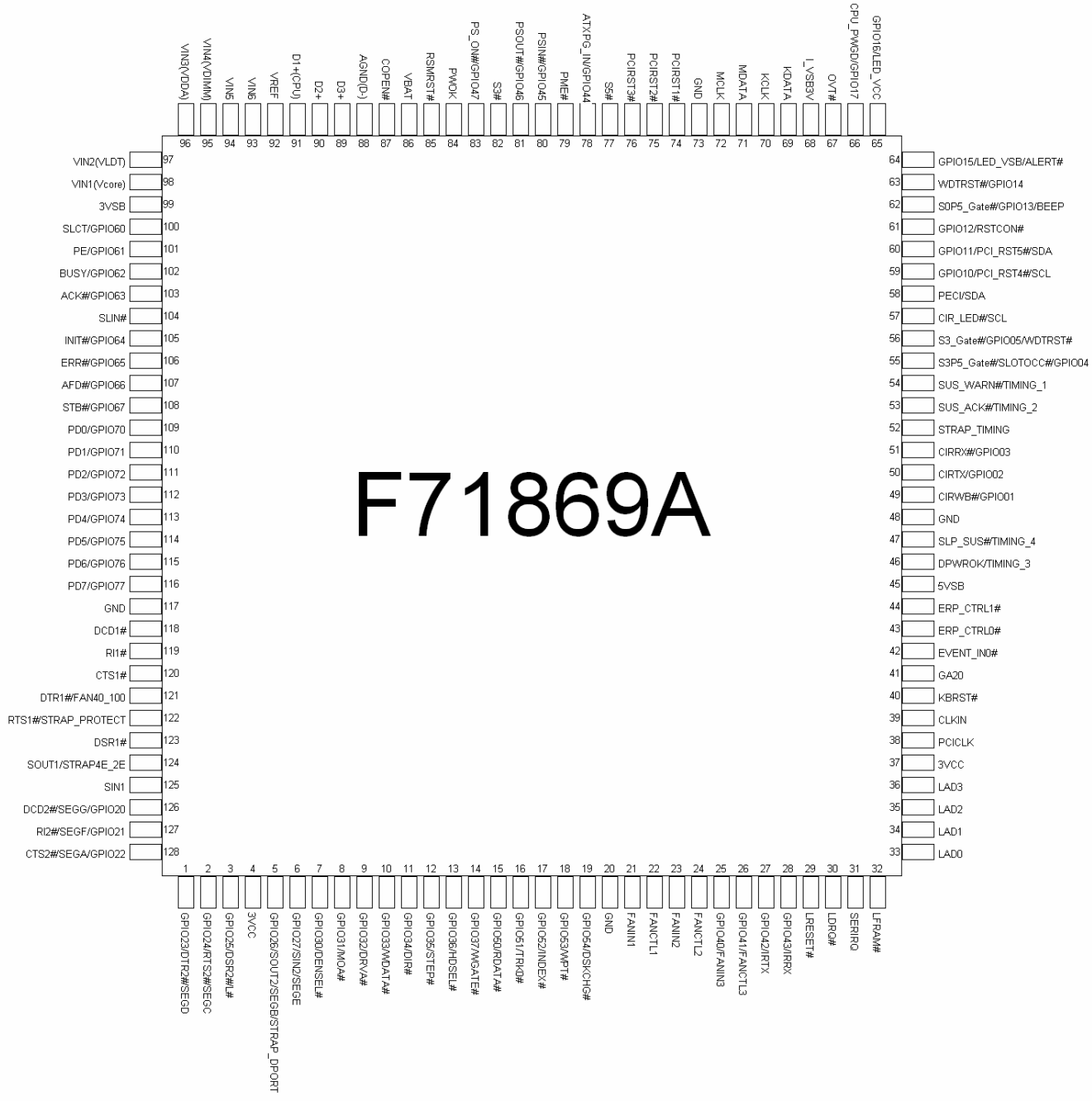


Figure1. F71869A pin configuration (14 *14)

4. Pin Description

$I/O_{12st-5v}$	- TTL level bi-directional pin with schmitt trigger, output with 12 mA sink capability, 5V tolerance.
$I/O_{16t-u47k}$	- TTL level bi-directional pin with 16 mA source-sink cap ability. With internal 47k pull-up.
I/OD_{12st5v}	- TTL level bi-directional pin with schmitt trigger, Open-drain output with 12 mA sink capability, 5V tolerance.
I/OD_{14st5v}	- TTL level bi-directional pin and schmitt trigger, Open-drain output with 14 mA sink capability, 5V tolerance.
I/OD_{16st5v}	- TTL level bi-directional pin with schmitt trigger, Open-drain output with 16 mA sink capability, 5V tolerance.
I/OOD_{12t}	- TTL level bi-directional pin, can be selected to OD or OUT by register, with 12 mA source-sink capability.
I/OOD_{12t5v}	- TTL level bi-directional pin, can select to OD or OUT by register, with 12 mA source-sink capability, 5V tolerance.
I/OOD_{8st5v}	- TTL level bi-directional pin and schmitt trigger, Open-drain output with 8 mA sink capability, 5V tolerance.
I/OOD_{12st5v}	- TTL level bi-directional pin and schmitt trigger, Open-drain output with 12 mA sink capability, 5V tolerance.
$I/OOD_{24st-5v}$	- TTL level bi-directional pin with schmitt trigger, can be selected to OD or OUT by register, with 24 mA sink capability, 5V tolerance.
I_{LV}/O_{D8-S1}	- Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.). Output with 8mA drive and 1mA sink capability.
OOD_{12-5v}	- OD or OUT selected by register with 12 mA sink capability, 5V tolerance.
OOD_{16-5v}	- OD or OUT selected by register with 16 mA sink capability, 5V tolerance.
O_{12}	- Output pin with 12 mA source-sink capability.
O_{16}	- Output pin with 16 mA source-sink capability.
O_{18}	- Output pin with 18 mA source-sink capability.
O_{20}	- Output pin with 20 mA source-sink capability.
O_{30}	- Output pin with 30 mA source-sink capability.
O_{12-5v}	- Output pin with 12 mA source-sink capability, 5V tolerance.
$O_{8t5v-u47k}$	- Output pin with 8 mA source-sink capability, pull-up 47k ohms, 5V tolerance.
OD_{12}	- Open-drain output pin with 12 mA sink capability.
OD_{14-5v}	- Open-drain output pin with 14 mA sink capability, 5V tolerance.
OD_{12-5v}	- Open-drain output pin with 12 mA sink capability, 5V tolerance.
OD_{24-5v}	- Open-drain output pin with 24 mA sink capability, 5V tolerance.
$OD_{12-5v-u10k}$	- Open-drain output pin with 12 mA sink capability, pull-up 10k ohms, 5V tolerance.
$OD_{16-5v-u10k}$	- Open-drain output pin with 16 mA sink capability, pull-up 10k ohms, 5V tolerance.
IN_{t5v}	- TTL level input pin,5V tolerance.
$IN_{st-u47k}$	- TTL level input pin and schmitt trigger. With internal pull-up 47k resistor.
IN_{st}	- TTL level input pin and schmitt trigger
IN_{st-lv}	- TTL low level input pin (VIH → 0.9V, VIL → 0.6V.)
IN_{st5v}	- TTL level input pin and schmitt trigger, 5V tolerance.
AIN	- Input pin(Analog).
AOUT	- Output pin(Analog).
P	- Power.

4.1 Power Pins

Pin No.	Pin Name	Type	Description
4,37	3VCC	P	Power supply voltage input with 3.3V (Support OVP)
45	5VSB(5VA)	P	5V stand by power input. Nomally the 5V stand by power source is from ATX Power directly.
68	I_VSB3V	P	3.3V internal standby power regulates from 5VSB, couple this pin with capacitor (0.1u) to ground for inter capacitance compensation. Besides, this pin can be an output pin to provide little current for Battery application when system enters ERP (G3' like) state. (Detail pleaser refer application circuit)
86	VBAT	P	Battery voltage input
88	AGND(D-)	P	Analog GND
99	3VSB	P	Analog Stand-by power supply voltage input 3.3V
20, 48, 73, 117	GND	P	Digital GND

4.2 LPC Interface

Pin No.	Pin Name	Type	PWR	Description
29	LRESET#	IN_{st5v}	VCC	Reset signal. It can connect to PCIRST# signal on the host.
30	LDRQ#	O_{16}	VCC	Encoded DMA Request signal.
31	SERIRQ	$I/O_{16t\text{-}u47k}$	VCC	Serial IRQ input/Output.
32	LFRAM#	$IN_{st\text{-}u47k}$	VCC	Indicates start of a new cycle or termination of a broken cycle.
33-36	LAD[0:3]	$I/O_{16t\text{-}u47k}$	VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
38	PCICLK	IN_{st}	VCC	33MHz PCI clock input.
39	CLKIN	IN_{st}	VCC	System clock input. According to the input frequency 24/48MHz.

4.3 FDC

Pin No.	Pin Name	Type	PWR	Description
7	GPIO30	I/OD_{14st5v}	I_VSB3V	Default General Purpose IO.
	DENSEL#	$OD_{14\text{-}5v}$		Drive Density Select. Set to 1 - High data rate.(500Kbps, 1Mbps) Set to 0 – Low data rate. (250Kbps, 300Kbps) FDC function is selected by register setting.
8	GPIO31	I/OD_{14st5v}	I_VSB3V	Default General Purpose IO.
	MOA#	$OD_{14\text{-}5v}$		Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output. FDC function is selected by register setting.
9	GPIO32	I/OD_{14st5v}	I_VSB3V	Default General Purpose IO.
	DRVA#	$OD_{14\text{-}5v}$		Drive Select A. When set to 0, this pin enables disk drive A.

				This is an open drain output. FDC function is selected by register setting.
10	GPIO33	I/OD_{14st5v}	I_VSB3V	Default General Purpose IO.
	WDATA#	OD_{14-5v}		Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output. FDC function is selected by register setting.
11	GPIO34	I/OD_{14st5v}	I_VSB3V	Default General Purpose IO.
	DIR#	OD_{14-5v}		Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion FDC function is selected by register setting.
12	GPIO35	I/OD_{14st5v}	I_VSB3V	Default General Purpose IO.
	STEP#	OD_{14-5v}		Step output pulses. This active low open drain output produces a pulse to move the head to another track. FDC function is selected by register setting.
13	GPIO36	I/OD_{14st5v}	I_VSB3V	Default General Purpose IO.
	HDSEL#	OD_{14-5v}		Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1 FDC function is selected by register setting.
14	GPIO37	I/OD_{14st5v}	I_VSB3V	Default General Purpose IO.
	WGATE#	OD_{14-5v}		Write enable. An open drain output. FDC function is selected by register setting.
15	GPIO50	I/OOD_{12st5v}	I_VSB3V	Default General Purpose IO. Support volume up control from LPC (Suppot scan code setting).
	RDATA#	IN_{st5v}		The read data input signal from the FDD. FDC function is selected by register setting.
16	GPIO51	I/OOD_{12st5v}	I_VSB3V	Default General Purpose IO. Support volume down control from LPC (Suppot scan code setting).
	TRK0#	IN_{st5v}		Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. FDC function is selected by register setting.
17	GPIO52	I/OOD_{12st5v}	I_VSB3V	Default General Purpose IO. Support mute control from LPC (Suppot scan code setting).
	INDEX#	IN_{st5v}		This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. FDC function is selected by register setting.
18	GPIO53	I/OOD_{12st5v}	I_VSB3V	Default General Purpose IO. Support PWM up for FANCTL3 (Suppot scan code setting).
	WPT#	IN_{st5v}		Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. FDC function is selected by register setting.
19	GPIO54	I/OOD_{12st5v}	I_VSB3V	Default General Purpose IO. Support PWM down for FANCTL3 (Suppot scan code setting).

	DSKCHG#	IN_{st5v}		Diskette change. This signal is active low at power on and whenever the diskette is removed. FDC function is selected by register setting.

4.4 UART and SIR

Pin No.	Pin Name	Type	PWR	Description
27	GPIO42	I/OOD_{12t5v}	VCC	Default General Purpose IO.
	IRTX	O_{12}		Infrared Transmitter Output. The function is selected by register setting.
28	GPIO43	I/OOD_{12t5v}	VCC	Default General Purpose IO.
	IRRX	IN_{st5v}		Infrared Receiver input. The function is selected by register setting.
118	DCD1#	IN_{st5v}	VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
119	RI1#	IN_{st5v}	I_VSB3V	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
120	CTS1#	IN_{st5v}	VCC	Clear To Send is the modem control input.
121	DTR1#	$O_{8t5v-u47k}$	VCC	UART 1 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. Internal 47k ohms pulled high and disable after power on strapping.
	FAN40_100	IN_{t5v}		Power on strapping pin: 1(Default): (Internal pull high) Power on fan speed default duty is 40%.(PWM) 0: (External pull down) Power on fan speed default duty is 100%.(PWM)
122	RTS1#	$O_{8t5v-u47k}$	VCC	UART 1 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
	STRAP_PROTECT	IN_{t5v}		Power on Strapping pin for anti surge protection function. 1: default is disabled alarm mode. Voltage protection function is enabled via setting the related register. 0: Force mode which is always enabled after power on.
123	DSR1#	IN_{st5v}	VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
124	SOUT1	$O_{8t5v-u47k}$	VCC	UART 1 Serial Output. Used to transmit serial data out to the communication link. Internal 47k ohms pulled high and disable after power on strapping.
	STRAP4E_2E	IN_{t5v}		Power on strapping: 1(Default): Configuration register 4E 0: Configuration register 2E
125	SIN1	IN_{st5v}	VCC	Serial Input. Used to receive serial data through the communication link.
126	DCD2#	IN_{st5v}	VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier. The function is selected by register setting.

	SEGG	O_{18}		SEGG for 7-segment display. (Select by pin 5 power on strapping)
	GPIO20	I/OOD_{8st5v}		Default General Purpose IO.
127	RI2#	IN_{st5v}	I_VSB3V	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set. The function is selected by register setting.
	SEGF	O_{18}		SEGF for 7-segment display. (Select by pin 5 power on strapping)
	GPIO21	I/OOD_{8st5v}		Default General Purpose IO.
128	CTS2#	IN_{st5v}	VCC	Clear To Send is the modem control input. The function is selected by register setting.
	SEGA	O_{18}		SEGA for 7-segment display. (Select by pin 5 power on strapping)
	GPIO22	I/OOD_{8st5v}		Default General Purpose IO.
1	GPIO23	I/OOD_{8st5v}	VCC	Default General Purpose IO.
	DTR2#	$O_{8t5v-u47k}$		UART 2 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. The function is selected by register setting.
	SEGD	O_{18}		SEGD for 7-segment display. (Select by pin 5 power on strapping)
2	GPIO24	I/OOD_{8st5v}	VCC	Default General Purpose IO.
	RTS2#	$O_{8t5v-u47k}$		UART 2 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. The function is selected by register setting.
	SEGC	O_{18}		SEGC for 7-segment display. (Select by pin 5 power on strapping)
3	GPIO25	I/OOD_{8st5v}	VCC	Default General Purpose IO.
	DSR2#	IN_{st5v}		Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. The function is selected by register setting.
	L#	O_{30}		L# for 7-segment display. (Select by pin 5 power on strapping)
5	GPIO26	I/OOD_{8st5v}	VCC	Default General Purpose IO.
	SOUT2	$O_{8t5v-u47k}$		UART 2 Serial Output. Used to transmit serial data out to the communication link. The function is selected by register setting.
	SEGB	O_{18}		SEGB for 7-segment display. (Select by pin 5 power on strapping)
	STRAP_DPORT	IN_{t5v}		Strap for 80 Port. Default internal Pull High for 80 Port Enable.
6	GPIO27	I/OOD_{8st5v}	VCC	Default General Purpose IO.
	SIN2	IN_{st5v}		Serial Input. Used to receive serial data through the communication link. The function is selected by register setting.

	SEGE	O_{18}		SEGE for 7-segment display. (Select by pin 5 power on strapping)

4.5 Parallel Port

Pin No.	Pin Name	Type	PWR	Description
100	SLCT	IN_{st5v}	VCC	An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
	GPIO60	I/OOD_{12t5v}		Default General Purpose IO.
101	PE	IN_{st5v}	VCC	An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	GPIO61	I/OOD_{12t5v}		Default General Purpose IO.
102	BUSY	IN_{st5v}	VCC	An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
	GPIO62	I/OOD_{12t5v}		Default General Purpose IO.
103	ACK#	IN_{st5v}	VCC	An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	GPIO63	I/OOD_{12t5v}		Default General Purpose IO.
104	SLIN#	I/OOD_{12st5v}	VCC	Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
105	INIT#	I/OOD_{12st5v}	VCC	Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	GPIO64	I/OOD_{12t5v}		Default General Purpose IO.
106	ERR#	IN_{st5v}	VCC	An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	GPIO65	I/OOD_{12t5v}		Default General Purpose IO.
107	AFD#	I/OOD_{12st5v}	VCC	An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	GPIO66	I/OOD_{12t5v}		Default General Purpose IO.
108	STB#	I/OOD_{12st5v}	VCC	An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.

	GPIO67	I/OOD_{12t5v}		Default General Purpose IO.
109	PD0	I/O_{12st5v}	VCC	Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	GPIO70	I/OOD_{12t5v}		Default General Purpose IO.
110	PD1	I/O_{12st5v}	VCC	Parallel port data bus bit 1.
	GPIO71	I/OOD_{12t5v}		Default General Purpose IO.
111	PD2	I/O_{12st5v}	VCC	Parallel port data bus bit 2.
	GPIO72	I/OOD_{12t5v}		Default General Purpose IO.
112	PD3	I/O_{12st5v}	VCC	Parallel port data bus bit 3.
	GPIO73	I/OOD_{12t5v}		Default General Purpose IO.
113	PD4	I/O_{12st5v}	VCC	Parallel port data bus bit 4.
	GPIO74	I/OOD_{12t5v}		Default General Purpose IO.
114	PD5	I/O_{12st5v}	VCC	Parallel port data bus bit 5.
	GPIO75	I/OOD_{12t5v}		Default General Purpose IO.
115	PD6	I/O_{12st5v}	VCC	Parallel port data bus bit 6.
	GPIO76	I/OOD_{12t5v}		Default General Purpose IO.
116	PD7	I/O_{12st5v}	VCC	Parallel port data bus bit 7.
	GPIO77	I/OOD_{12t5v}		Default General Purpose IO.

4.6 Hardware Monitor

Pin No.	Pin Name	Type	PWR	Description
93	VIN6	AIN	I_VSB3V	Voltage input 6. This pin support OVP function, and default is disable.
94	VIN5	AIN	I_VSB3V	Voltage input 5. This pin support OVP function, and default is disable.
95	VIN4 (VDIMM)	AIN	I_VSB3V	Voltage input 4 or VDIMM input used in AMD platform. The input voltage level for timing control usage must be over 1V after voltage divider.
96	VIN3 (VDDA)	AIN	I_VSB3V	Voltage input 3 or VDDA input used in AMD platform. The input voltage level for timing control usage must be over 1V after voltage divider.
97	VIN2 (VLDT)	AIN	I_VSB3V	Voltage input 2 or VLDT input used in AMD platform. The input voltage level for timing control usage must be over 1V after voltage divider.
98	VIN1 (Vcore)	AIN	I_VSB3V	Voltage Input for Vcore. The input voltage level for timing control usage must be over 0.7V.
21	FANIN1	IN_{st5v}	VCC	Fan 1 tachometer input.
22	FANCTL1	$OOD_{12\text{-}5v}$ AOUT	VCC	Fan 1 control output. It is also a trap pin to select a PWM or a DAC output, except being an output pin. It defaults to be a voltage output by pulling down internally. It is set as a PWM output as connected a 4.7K resistor and pulled high to 3.3V.
23	FANIN2	IN_{st5v}	VCC	Fan 2 tachometer input.
24	FANCTL2	$OOD_{12\text{-}5v}$	VCC	Fan 2 control output. It is also a trap pin to select a PWM or

		AOUT		a DAC output, except being an output pin. It defaults to be a voltage output by pulling down internally. It is set as a PWM output as connected a 4.7K resistor and pulled high to 3.3V.
25	GPIO40	I/OOD_{12st5v}	VCC	Default General Purpose IO.
	FANIN3	IN_{st5v}		Fan 3 speed input. This function is selected by register setting.
26	GPIO41	I/OOD_{12st5v}	VCC	Default General Purpose IO. This pin default function is GPIO function. Please take care the application if user wants to implement FANCTL function.
	FANCTL3	OOD_{12-5v} AOUT		Fan 3 control output. It is also a trap pin to select a PWM or a DAC output, except being an output pin. It defaults to be a voltage output by pulling down internally. It is set as a PWM output as connected a 4.7K resistor and pulled high to 3.3V. The PWM output frequency can be programmed to 220Hz for LCD backlight control.
57	CIR_LED#	OD_{12-5v}	I_VSB3V	LED for CIR to indicate receiver is receiving data.
	SCL	I/OD_{12ts5v}		SMBUS Interface CLOCK pin.
58	PECI	I_{LV}/O_{D8-S1}	I_VSB3V	Intel PECI hardware monitor interface. When TIMING_GPIO pin is set in GPIO function (INTEL mode). PECI function can be set by the register.
	SDA	I/OD_{12ts5v}		SMBUS Interface DATA pin.
63	WDTRST#	OD_{12-5v}	I_VSB3V	Watch dog timer signal output.
	GPIO14	I/OOD_{12st5v}		General Purpose IO. GPIO function is selected by register setting
67	OVT#	OD_{12-5v}	I_VSB3V	Over temperature signal output.
79	PME#	OD_{12-5v}	I_VSB3V	Generated PME event. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the S3 state.
89	D3+	AIN	I_VSB3V	Thermal diode/transistor temperature sensor input for system use.
90	D2+	AIN	I_VSB3V	Thermal diode/transistor temperature sensor input.
91	D1+(CPU)	AIN	I_VSB3V	CPU thermal diode/transistor temperature sensor input. This pin is for CPU use.
92	VREF	AOUT	I_VSB3V	Voltage sensor output.

4.7 ACPI Function Pins

Pin No.	Pin Name	Type	PWR	Description
59	GPIO10	I/OOD_{12st5v}	I_VSB3V	Default General Purpose IO. GPIO function is selected by register setting
	PCI_RST4#	O_{12-5v}		It is an output buffer of LRESET#. This function is selected by register setting.
	SCL	I/OD_{12ts5v}		SMBUS Interface CLOCK pin.
60	GPIO11	I/OOD_{12st5v}		Default General Purpose IO.

	PCI_RST5#	$O_{12\text{-}5v}$	I_VSB3V	It is an output buffer of LRESET#. This function is selected by register setting.
	SDA	I/OD_{12ts5v}		SMBUS Interface DATA pin.
61	GPIO12	I/OOD_{12st5v}	I_VSB3V	Default General Purpose IO.
	RSTCON#	IN_{st5v}		It is an output buffer of RSTCON#. This function is selected by register setting.
64	GPIO15	I/OOD_{12st5v}	I_VSB3V	Default General Purpose IO.
	LED_VSB	$OD_{12\text{-}5v}$		Power LED for VSB. This function is selected by register setting.
	ALERT#	$OD_{12\text{-}5v}$		Alert a signal when temperature over limit setting. This function is selected by register setting.
65	GPIO16	I/OOD_{12st5v}	I_VSB3V	Default General Purpose IO.
	LED_VCC	$OD_{12\text{-}5v}$		Power LED for VCC. This function is selected by register setting.
66	CPU_PWGD	$OD_{12\text{-}5v}$	I_VSB3V	CPU Power Good signal output (Detected by VIN1~VIN4 level good)
	GPIO17	I/OOD_{12st5v}		General Purpose IO. GPIO function is selected by register setting
74	PCIRST1#	$OD_{12\text{-}5v}$	I_VSB3V	It is an output buffer of LRESET#.
75	PCIRST2#	$O_{12\text{-}5v}$	I_VSB3V	It is an output buffer of LRESET#.
76	PCIRST3#	$O_{12\text{-}5v}$	I_VSB3V	It is an output buffer of LRESET#.
77	S5#	IN_{st5v}	I_VSB3V	S5# signal input.
78	ATXPG_IN	IN_{st5v}	I_VSB3V	ATX Power Good input.
	GPIO44	I/OOD_{12st5v}		General Purpose IO. GPIO function is selected by register setting.
80	PSIN#	IN_{ts5v}	I_VSB3V	Main power switch button input.
	GPIO45	I/OOD_{12st5v}		General Purpose IO. GPIO function is selected by register setting.
81	PSOUT#	$OD_{12\text{-}5v}$	I_VSB3V	Panel Switch Output. This pin is low active and pulse output. It is power on request output#.
	GPIO46	I/OOD_{12st5v}		General Purpose IO. GPIO function is selected by register setting.
82	S3#	IN_{st5v}	I_VSB3V	S3# Input is Main power on-off switch input.
83	PS_ON#	$OD_{12\text{-}5v}$	I_VSB3V	Power supply on-off control output. Connect to ATX power supply PS_ON# signal.
	GPIO47	I/OOD_{12st5v}		General Purpose IO. GPIO function is selected by register setting.
84	PWOK	$OD_{12\text{-}5v}$	VBAT	PWOK function, It is power good signal of VCC, which is delayed 400ms (default) as VCC arrives at 2.8V.
85	RSMRST#	$OD_{12\text{-}5v\text{-}u10k}$	VBAT	Resume Reset# function, It is power good signal of VSB, which rises delayed 66ms as VSB arrives at 2.8V and falls as VSB drops to 2.6V. There is an option to set RSMRST# rises at 3.05V and falls at 2.95V.
87	COPEN#	IN_{st5v}	VBAT	Case Open Detection #. This pin is connected to a specially designed low power CMOS flip-flop backed by the battery for case open state preservation during power

				loss.

4.8 Power Saving and Others

Pin No.	Pin Name	Type	PWR	Description
42	EVENT_IN0#	IN_{ts5v}	I_VSB3V	Wake-up event input. The signal input wakes the system up from the sleep state.
43	ERP_CTRL0#	OD_{12}	I_VSB3V	Standby power rail control pin 0. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.
44	ERP_CTRL1#	OD_{12}	I_VSB3V	Standby power rail control pin 1. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.
46	DPWROK	$OD_{12\text{-}5v}$	I_VSB3V	Resume Reset# function, It is power good signal of VSB, which is delayed 66ms as VSB arrives at 4.4V. Couple this pin to PCH when system supports Intel DSW state function.
	TIMING_3	$OD_{12\text{-}5v}$		Active high. Timing sequence 3 of power on/off sequence pins. The external pull high resistor is required. (Detected by VIN3 level good)
47	SLP_SUS#	$IN_{st\text{-}lv}$	I_VSB3V	For Intel CPT DSW function. Connect to PCH SLP_SUS pin.
	TIMING_4	$OD_{12\text{-}5v}$		Active high. Timing sequence 4 of power on/off sequence pins. The external pull high resistor is required. (Detected by VIN1 level good)
49	CIRWB#	IN_{ts5v}	I_VSB3V	CIR wide-band receiver input. (For Learning use)
	GPIO01	I/OOD_{12t}		General Purpose IO. GPIO function is selected by register setting
50	CIRTX#	O_{20}	I_VSB3V	CIR Transmitter to transmit data.
	GPIO02	I/OOD_{12t}		General Purpose IO. GPIO function is selected by register setting
51	CIRRX#	IN_{ts5v}	I_VSB3V	CIR long-range receiver input
	GPIO03	I/OOD_{12t}		General Purpose IO. GPIO function is selected by register setting
52	STRAP_TIMING	IN_{st5v}	I_VSB3V	Strap Pin for AMD and Intel Cougar Point timing. Internal pull high with AMD timing (Default).
53	SUS_ACK#	$OOD_{16\text{-}5v}$	I_VSB3V	This pin must wait SUS_WARN# signal for entering DSW power state.
	TIMING_2	$OD_{12\text{-}5v}$		Active high. Timing sequence 2 of power on/off sequence pins. The external pull high resistor is required. (Detected by VIN4 level good)
54	SUS_WARN#	IN_{ts5v}	I_VSB3V	This pin asserts low when the PCH is planning to enter the DSW power state. It can detect 5VDUAL level with delay setting supported.
	TIMING_1	$OD_{12\text{-}5v}$		Active high. Timing sequence 1 of power on/off sequence

				pins. The external pull high resistor is required. (Output detected by VCCOK(VDDOK) level good, ref Figure 15)
55	S_{3P5}_Gate#	OD_{12}	I_VSB3V	Status Pin2 for S0#/S3#/S5# states application. (Default function) In S0# → S_{3P5}_Gate# pin status is Tri-state. In S3# (S3P5_Gate # pin status is Low level. In S5# (S3P5_Gate # pin status is Tri-state, and can be programmed Low level.
	SLOTOCC#	IN_{ts5v}		CPU SLOTOCC# input.
	GPIO04	$OD_{12\text{-}5v}$		General Purpose IO. GPIO function is selected by register setting
56	S3_Gate#	OD_{12}	I_VSB3V	Status Pin1 for S0#/S3#/S5# states application. (Default function) In S0# (S3_Gate# pin status is Tri-state. In S3# (S3_Gate# pin status is Low level. In S5# (S3_Gate# pin status is Tri-state.
	GPIO05	I/OOD_{12st5v}		General Purpose IO. GPIO function is selected by register setting
	WDTRST#	$OD_{12\text{-}5v}$		Watch dog timer signal output.
62	S0P5_Gate#	$OD_{24\text{-}5v}$	I_VSB3V	S0P5_Gate# for S0#/S3#/S5# states application. In S0# (S0P5_Gate# pin status is Low-state. In S3# (S0P5_Gate# pin status is Tri-state. In S5# → S_{0P5}_Gate# pin status is Tri-state, and can be programmed Low-state.
	GPIO13	I/OOD_{24st5v}		General Purpose IO. GPIO function is selected by register setting
	BEEP	$OD_{24\text{-}5v}$		Beep pin.

4.9 KBC Function

Pin No.	Pin Name	Type	PWR	Description
40	KBRST#	$OD_{16\text{-}5v\text{-}u10k}$	VCC	Keyboard reset. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P20)
41	GA20	$OD_{16\text{-}5v\text{-}u10k}$	VCC	Gate A20 output. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P21)
69	KDATA	I/OD_{16st5V}	I_VSB3V	Keyboard Data.
70	KCLK	I/OD_{16st5V}	I_VSB3V	Keyboard Clock.
71	MDATA	I/OD_{16st5V}	I_VSB3V	PS2 Mouse Data.
72	MCLK	I/OD_{16st5V}	I_VSB3V	PS2 Mouse Clock.

5. Function Description

5.1 Power on Strapping Option

The F71869A provides eight pins for power on hardware strapping to select functions. There is a form to describe how to set the functions you want.

Table1. Power on trap configuration

Pin No.	Symbol	Value	Description
52	STRAP_TIMING	1	AMD Timing (Default)
		0	Intel Cougar Point Timing
121	FAN40_100	1	Power on Fan speed default duty is 40% (PWM) (Default)
		0	Power on Fan speed default duty is 100%(PWM)
124	STRAP4E_2E	1	Configuration Register I/O port is 4E/4F. (Default)
		0	Configuration Register I/O port is 2E/2F.
22	FANCTL1	1	FANCTRL1 is PWM mode. Connect a 4.7K resistor and pull high to 3.3V.
		0	FANCTLR1 is DAC mode. (Default)
24	FANCTL2	1	FANCTRL2 is PWM mode. Connect a 4.7K resistor and pull high to 3.3V.
		0	FANCTLR2 is DAC mode. (Default)
26	FANCTL3	1	FANCTRL3 is PWM mode. Connect a 4.7K resistor and pull high to 3.3V.
		0	FANCTLR3 is DAC mode. (Default)
5	STRAP_DPORT	1	Enable 80 Port (Default)
		0	Disable 80 Port
122	STRAP_PROTECT	1	Default is disabled alarm mode. Voltage protection function is enabled via setting the related register.
		0	Force mode which is always enabled after power on.

5.2 Hardware Monitor

For the 8-bit ADC has the 8mv LSB, the maximum input voltage of the analog pin is 2.048V. Therefore the voltage under 2.048V (ex: 1.5V) can be directly connected to these analog inputs. The voltage higher than 2.048V should be reduced by a factor with external resistors so as to obtain the input range. Only 3VCC/VSB/VBAT is an exception for it is main power of the F71869A. Therefore 3VCC/VSB/VBAT can directly connect to this chip's power pin and need no external resistors. There are two functions in this pin with 3.3V. The first function is to supply internal analog power of the F71869A and the second function is that voltage with 3.3V is connected to internal serial resistors to monitor the +3.3V voltage. The internal serial resistors are two 150K ohm, so that the internal reduced voltage is half of +3.3V.

There are four voltage inputs in the F71869A and the voltage divided formula is shown as follows:

$$VIN = V_{+12V} \times \frac{R_2}{R_1 + R_2}$$ where V_{+12V} is the analog input voltage, for example.

If we choose R1=27K, R2=5.1K, the exact input voltage for V+12v will be 1.907V, which is within the tolerance. As for application circuit, it can be refer to the figure shown as follows.

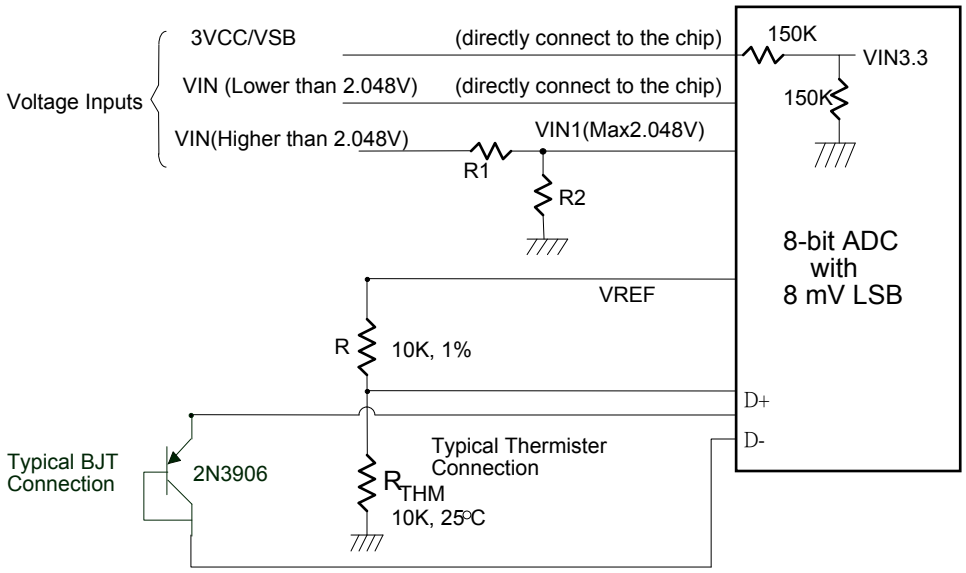


Figure 2. Hardware monitor configuration

The F71869A monitors three remote temperature sensors. These sensors can be measured from -40°C to 127°C. More detail please refer register description.

Table 2. Remote-sensor transistor manufacturers

Manufacturer	Model Number
Panasonic	2SB0709 2N3906
Philips	PMBT3906

5.2.1. Table Range:

Table 3. Display range is from -40°C to 127°C in 2's complement format.

Temperature	Digital Output
-40°C	1101 1000
-1°C	1111 1111
1°C	0000 0001
90°C	0101 1010

127°C	1111 1111
Open	1000 0000

5.2.2. Monitor Temperature from "Thermistor"

The F71869A can connect three thermistors to measure environment temperature or remote temperature. The specification of thermistor should be considered to (1) (value is 3435K (2) resistor value is 10K ohm at 25(C. In the Figure 2, the thermistor is connected by a serial resistor with 10K ohm, then being connected to VREF.

5.2.3. Monitor Temperature from "Thermal diode"

Also, if the CPU, GPU or external circuits provide thermal diode for temperature measurement, the F71869A is capable to these situations. The build-in reference table is for PNP 2N3906 transistor. In the Figure 2, the transistor is directly connected into temperature pins.

5.2.4. ADC Noise Filtering

The ADC is integrating type with inherently good noise rejection. Micro-power operation places constraints on high-frequency noise rejection; therefore, careful PCB board layout and suitable external filtering are required for high-accuracy remote measurement in electronically noisy environment. High frequency EMI is best filtered at D+ and D- with an external 2200pF capacitor. Too high capacitance may introduce errors due to the rise time of the switched current source. Nearly all noise sources tested cause the ADC measurement to be higher than the actual temperature, depending on the frequency and amplitude.

5.2.5. Monitor Temperature from "SMBus device"

F71869A provides SMBus block read/write compatible Platform Control Hub (PCH) EC SMBus protocol, and provides byte read/write protocol to read CPU and chipset thermal temperature information. For byte read /write protocol, F71869A supports 4-suit device address to read or write from device information. For block read/write, F71869A support 1 suits device address and maximum 17 byte count for read protocol to read from device information, and 4 byte count for write protocol to write information to device.

5.2.6. Monitor Temperature from "PECI"

F71869A support Intel PECI1.1/PECI3.0/PECI_Request/PECI_Available

interfaces to read temperature from PECI device.

5.2.7. Temperature OVT# Signal

There is a mode of temperature (t1 to t4) OVT function, and refer t1 to t4 temperature in the below Figure.

Over temperature event will trigger OVT# that shown as figure 3. In hysteresis mode, when monitored temperature exceeds the high temperature threshold value, OVT# will be asserted until the temperature goes below the hysteresis temperature.

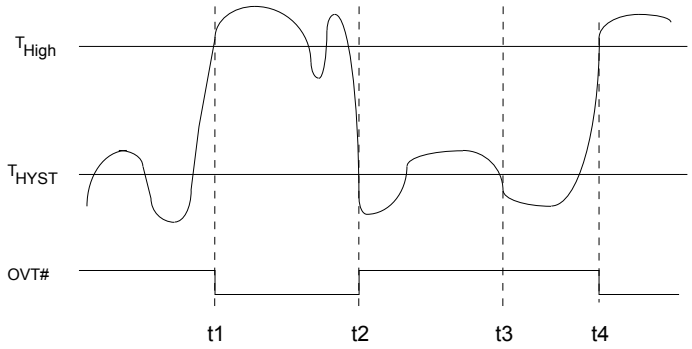
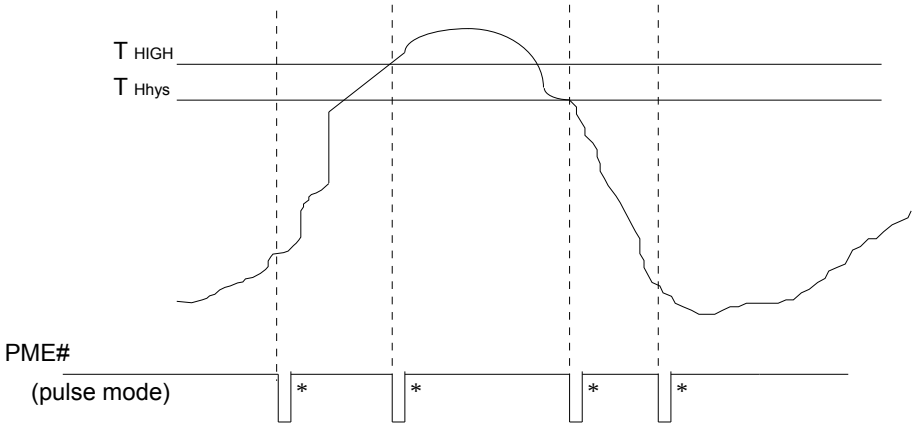


Figure 3

5.2.8. Temperature PME#

PME# interrupt for temperature is shown as figure 4. Temperature exceeding high limit (low limit) or going below high hysteresis (low hysteresis) will cause an interrupt if the previous interrupt has been reset by writing “1” all the interrupt Status Register.



*Interrupt Reset when Interrupt Status Registers are written 1

Figure 4 Hysteresis mode illustration

5.2.9. Fan Speed Count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over 5V. If the input signals from the tachometer outputs are over the 5V, the external trimming circuit should be added to reduce the voltage to obtain the input specification.

Determine the fan counter according to:

$$\text{Count} = \frac{1.5 \times 10^6}{\text{RPM}}$$

In other words, the fan speed counter has been read from register, the fan speed can be evaluated by the following equation. As for fan, it would be best to use 2 pulses tachometer output per round.

$$\text{RPM} = \frac{1.5 \times 10^6}{\text{Count}}$$

As the register description of datasheet, the parameter “Count” register provides 12-bit resolution for RPM counting. In Fintek design, the value of parameter “Count” is from 4096 ~ 64 (5 bit filter). Therefore the RPM measure capability is from 366 ~ 23438 rpm.

Above example is for 2 pulses tachometer (Normal 4 Phases fan) output per round. If you use 8 Phases fan, means output 4 pulses per round. The RPM measure capability is from 183 ~ 11719 rpm.

5.2.10. Fan Speed Control

The F71869A provides 2 fan speed control methods: one is DAC FAN control and the other is PWM duty cycle.

1. DAC Fan Control

The range of DC output is 0~3.3V, controlled by 8-bit register. 1 LSB is about 0.013V. The output DC voltage is amplified by external OP circuit, thus to reach maximum FAN OPERATION VOLTAGE, 12V. The output voltage will be given as followed:

$$\text{Output_voltage (V)} = 3.3 \times \frac{\text{Programmed 8bit Register Value}}{255}$$

And the suggested application circuit for DAC fan control would be:

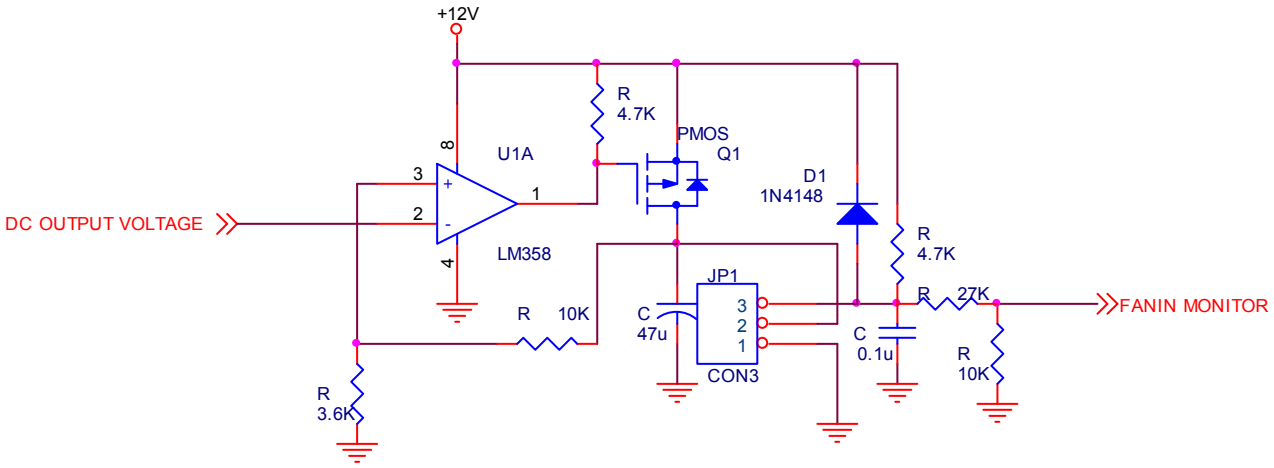


Figure 5 DAC fan control application circuit

2. PWM duty Fan Control

The duty cycle of PWM can be programmed by a 8-bit register. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty_cycle(\%)} = \frac{\text{Programmed 8bit Register Value}}{255} \times 100\%$$

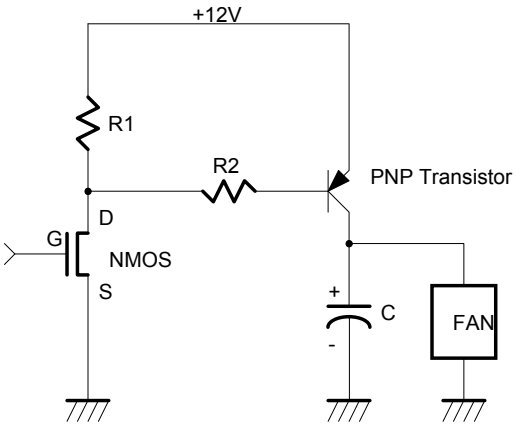


Figure 6 +12/5V PWM fan control application circuit

5.2.11. Fan Speed Control Mechanism

There are some modes to control fan speed and they are 1.Manual mode, 2.Stage auto mode 3. Linear auto mode. More detail, please refer the description of registers.

Each fan can be controlled by up to 8 kinds of temperature inputs: (1) D1+ temperature (2) D2+ temperature (3) D3+ temperature (4) PECI temperature (5) 4 suits SMBus master temperature. Each fan would make the maximum temperature comparison form those inputs with the expected speed, and decide the suitable fan speed. Please refer below figure 7.

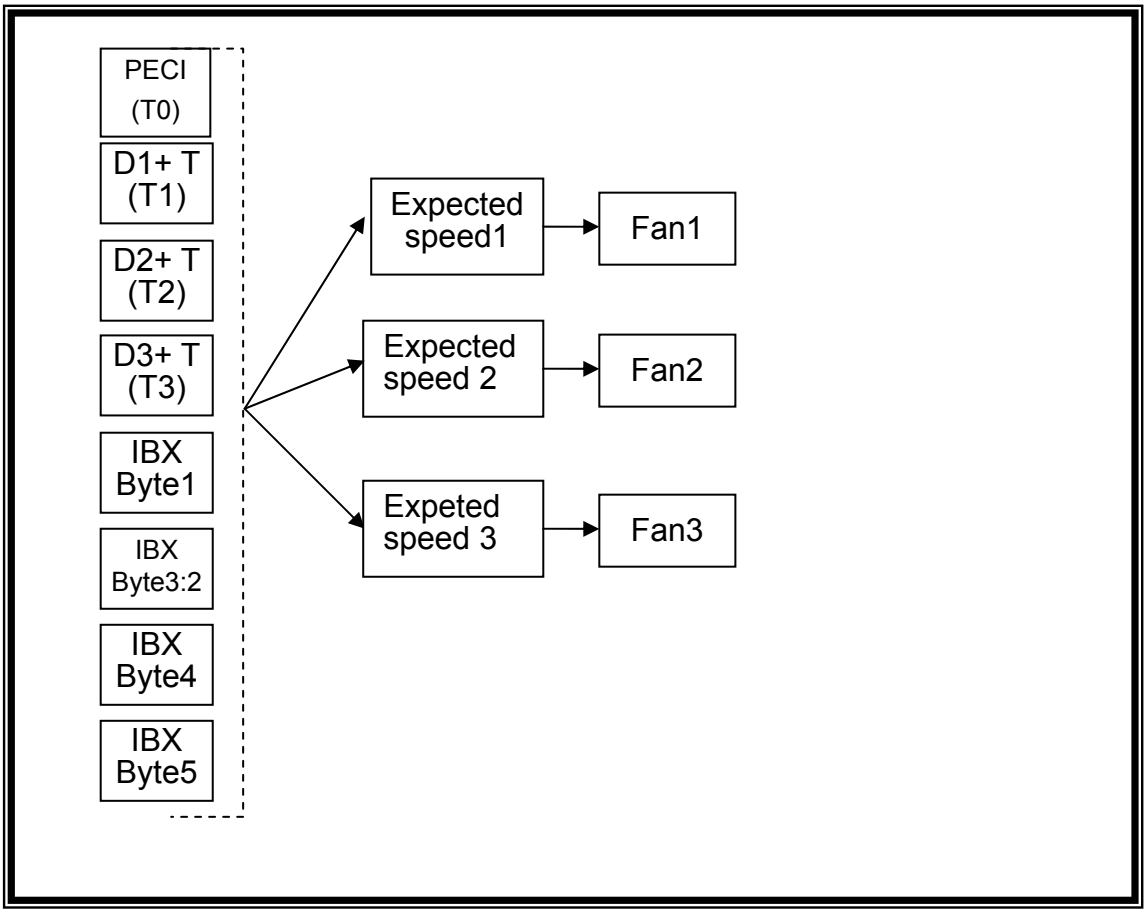


Figure 7 Relative temperature fan control

Manual mode

For manual mode, it generally acts as software fan speed control.

Auto mode

In auto mode, the F71869A provides automatic fan speed control related to temperature variation of CPU/GPU or the system. The F71869A can provide four temperature boundaries and five intervals, and each interval has its related fan speed count. All these values should be set by BIOS first. Take FAN1 for example, the 4 temperature boundaries could be set from register 0xA6 to 0xA9 and the five intervals for fan speed control could be set from register 0xAA to 0xAE. And the

hysteresis setting (0 ~ 15°C) could also be found in register 0x98.

The Manual Mode and Auto Mode could be selected by register 0x96h.

There are two kinds of auto mode: stage auto mode and linear auto mode. The “FAN1_ INTERPOLATION_EN” in register 0xAFh is used for linear auto mode enable. The following examples explain the differences for stage auto mode and linear auto mode.

Stage auto mode

In this mode, the fan keeps in a same speed for each temperature interval. And there are two types of fan speed setting: PWM Duty and RPM %.

A. Stage auto mode (PWM Duty)

Set the temperature limits as 70°C, 60°C, 50°C, 40°C and the duty as 100%, 90%, 80%, 70%, 60%

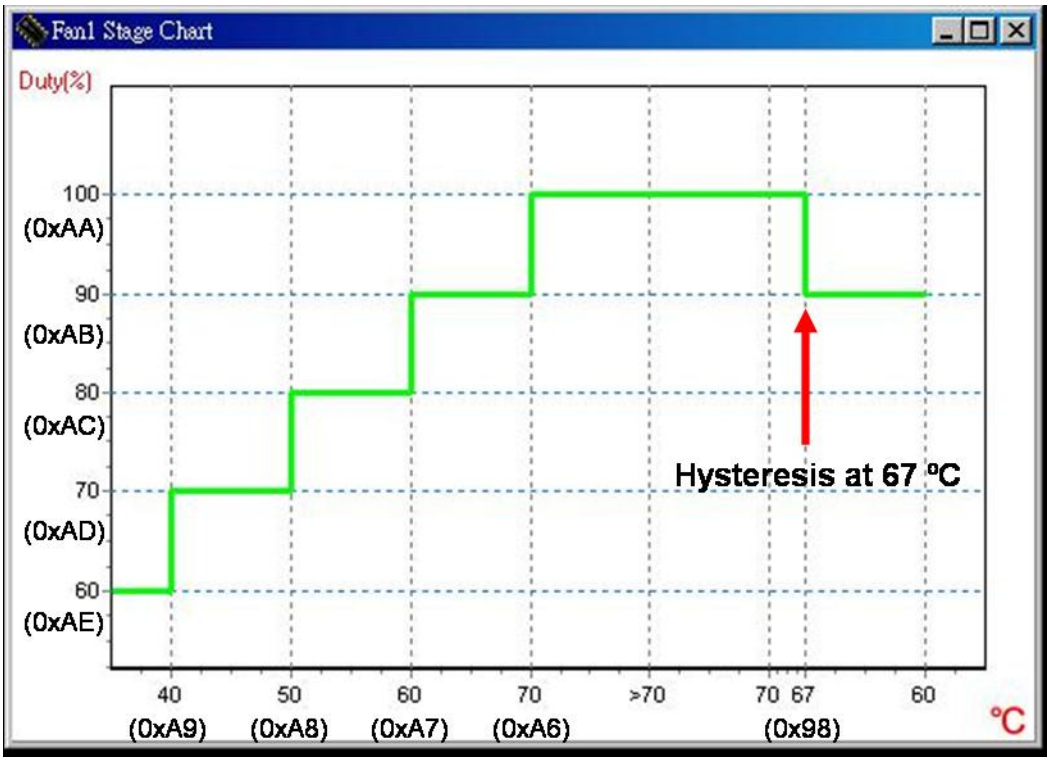


Figure 8 Stage mode fan control illustration-2

a. Once the temperature is under 40°C, the lowest fan speed keeps in the 60% PWM duty.
b. Once the temperature is over 40°C, 50°Cand 60°C, the fan speed will vary from 70%, 80% to 90% PWM duty and increasing with the temperature level.
c. For the temperature higher than 70°C, the fan speed keeps in 100% PWM duty.
d. If set the hysteresis is 3°C (default 4°C), once the temperature becomes lower than 67°C, the fan speed would reduce to 90% PWM duty.

B. Stage auto mode (RPM%)

Set the temperature as 70°C, 60°C, 50°C, 40°C and the corresponding fan speed is 6,000 rpm,

5,400 rpm, 4,800 rpm, 4,200 rpm, and 3,600 rpm (assume the Max Fan Speed is 6,000 rpm).

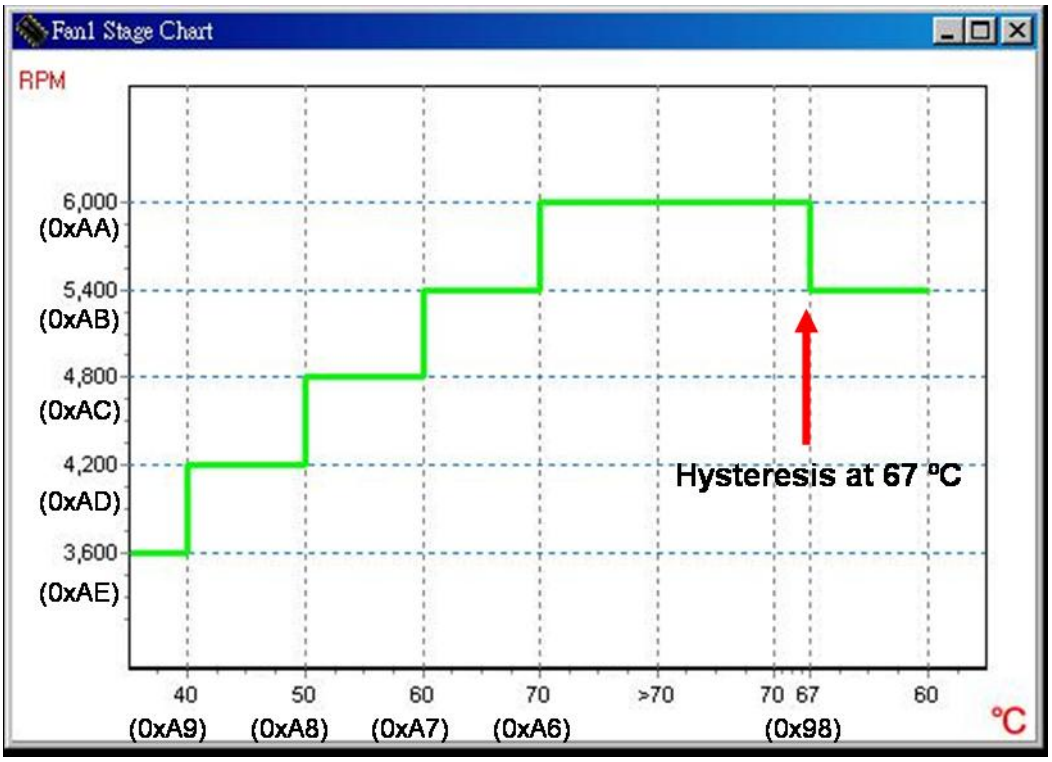


Figure 9 Stage mode fan control illustration-3

a. Once the temperature is lower than 40°C, the lowest fan speed keeps in 3,600 rpm (60% of full speed).
b. Once the temperature is higher than 40°C, 50°C and 60°C, the fan speed will vary from 4,200 rpm to 5,400 rpm and increasing with the temperature level.
c. For the temperature higher than 70°C, the fan speed keeps in the full speed 6,000 rpm.
d. If the hysteresis is set as 3°C (default 4°C), once temperature gets lower than 67°C, the fan speed would reduce to 5,400 rpm.

Linear auto mode

F71869A also supports linear auto mode. The fan speed would increase or decrease linearly with the temperature. There are also PWM Duty and RPM% modes for it.

A. Linear auto mode (PWM Duty)

Set the temperature as 70°C, 60°C, 50°C and 40°C and the duty is 100%, 80%, 70%, 60% and 50%.

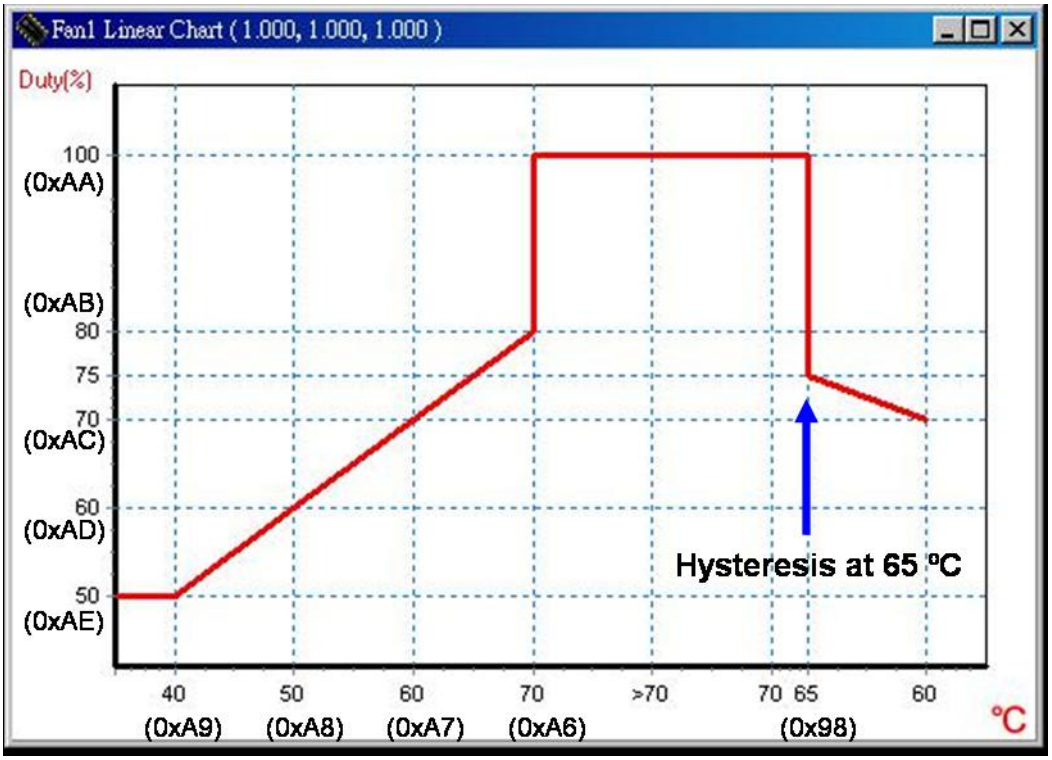


Figure 10 Linear mode fan control illustration-1

a. Once the temperature is lower than 40°C, the lowest fan speed keeps in the 50% PWM duty
b. Once the temperature becomes higher than 40°C, 50°C and 60°C, the fan speed will vary from 50% to 80% PWM duty linearly with the tempreature variation. The temp.-fan speed monitoring flash interval is 1sec.
c. Once the temperature goes over 70°C, the fan speed will directly increase to 100% PWM duty (full speed).
d. If set the hysteresis is 5°C (default is 4°C), once the temperature becomes lower than 65°C (instead of 70°C), the fan speed will reduce from 100% PWM duty and decrease linearly with the temperature.

B. Linear auto mode (RPM%)

Set the temperature as 70°C, 60°C, 50°C, 40°C and the corresponding fan speed is 6,000 rpm, 4,800 rpm, 4,200 rpm, 3,600 rpm and 3,000 rpm (assume the Max Fan Speed is 6,000 rpm).

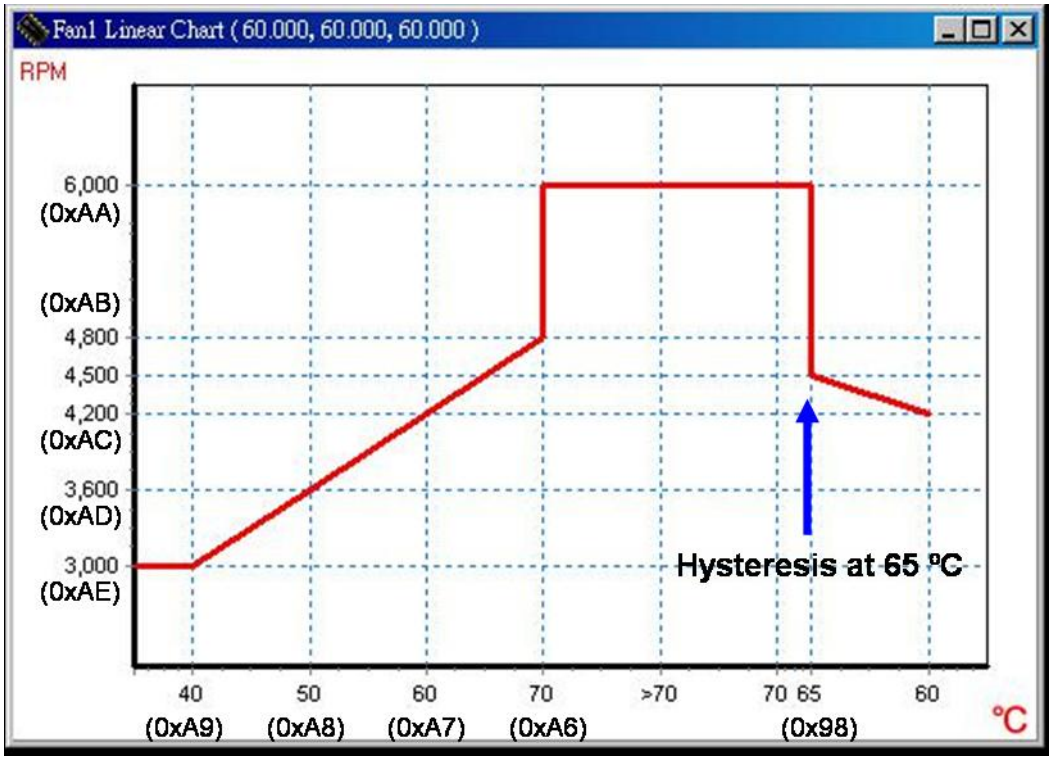
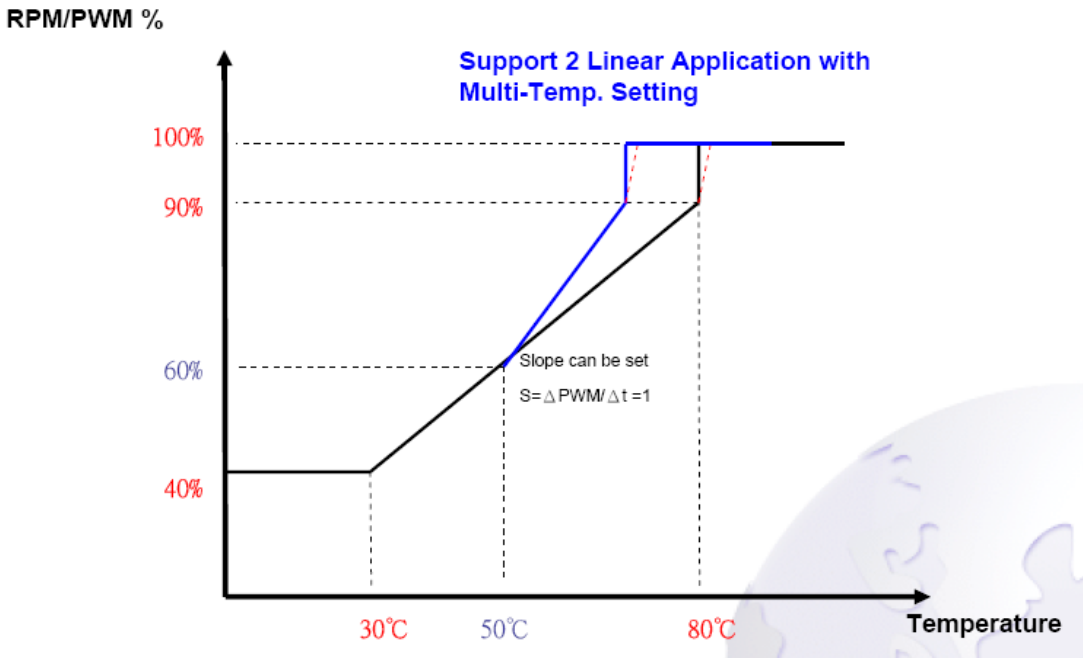


Figure 11 Linear mode fan control illustration-2

a. Once the temperature is lower than 40°C, the lowest fan speed keeps in 3,000 rpm (50% of full speed).
b. Once the temperature is over 40°C,50°C and 60°C, the fan speed will vary from 3,000 to 4,800 rpm almost linearly with the temperature variation because the temp.-fan speed monitoring flash interval is 1sec.
c. Once the temperature goes over 70°C, the fan speed will directly increase to full speed 6,000 rpm.
d. If the hysteresis is 5°C (default is 4°C), once the temperature becomes lower than 65°C (instead of 70°C), the fan speed wull reduce from full speed and decrease linearly with the temperature.

Fan Speed Control with Multi-temperature.

F71869A supports Multi-temperature for one fan control. This function works with linear auto mode can extend two linear slopes for one Fan control. As the graph below, this machine can support more silence fan control in low temperature environment and faster fan speed in high temperature segment. More detail setting please refers to the registers.

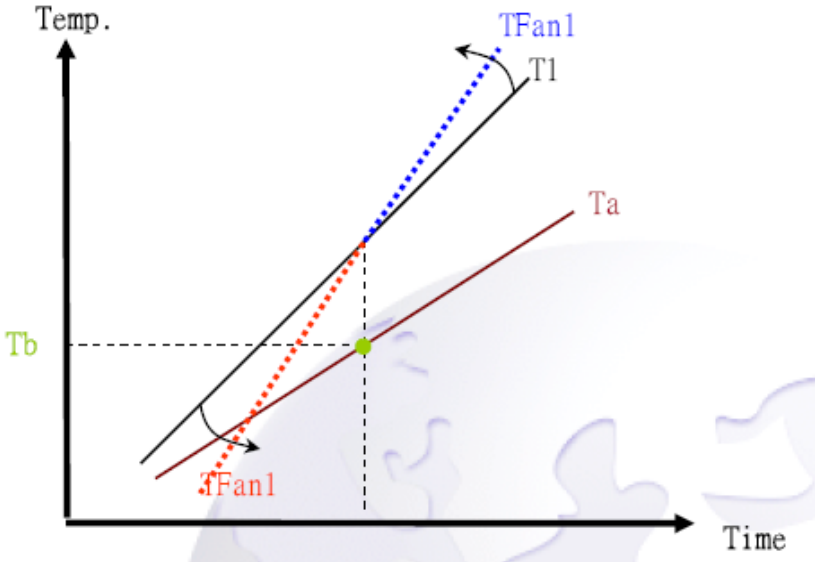


In the figure below, TFan1 is the scaled temperature for fan1. T1 is the real temperature for the fan1 sensor. Ta is another temperature data which can be used for linearly scale up or scale down the fan1 speed curve. Tb would be the point which starts the temperature scaling. The slope for the temperature curve over and under Tb would be Ctup and Ctdn.

TFan1= T1 + (Ta-Tb)*Ctup

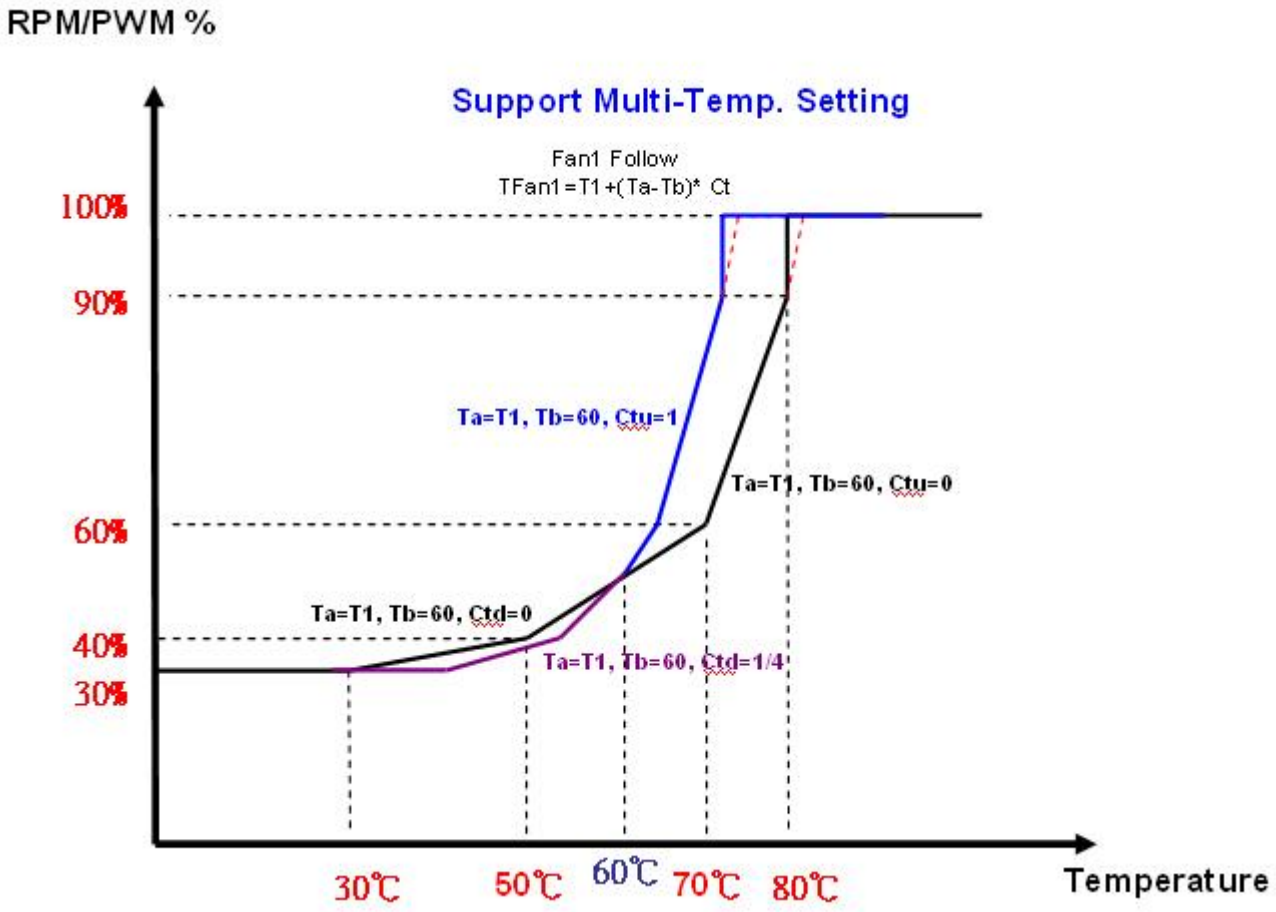
TFan1= T1 + (Ta-Tb)*Ctdn

1. **Ctup**, **Ctdn** Can be Programmed to **1, ½, ¼, 0**
2. **Ta** Can be Selected to the Same Temp. Source (Ex:T1)



In application, we can set the Ta as the 2nd sensor temperature and Tb as the temperature which starts the scaling. So if the 2nd sensor temperature Ta is higher or lower than Tb, the fan1 speed would be changed with it.

EX: Ta = T1, Tb = 60, Ctu = 1, Ctd = 1/4



5.2.12. FAN_FAULT#

Fan_Fault# will be asserted when the fan speed doesn't meet the expected fan speed within a programmable period (default is 11 seconds) or when fan stops with respect to PWM duty-cycle which should be able to turn on the fan. There are two conditions may cause the FAN_FAULT# event.

(1). When PWM_Duty reaches 0xFF, the fan speed count can't reach the fan expected count in time.

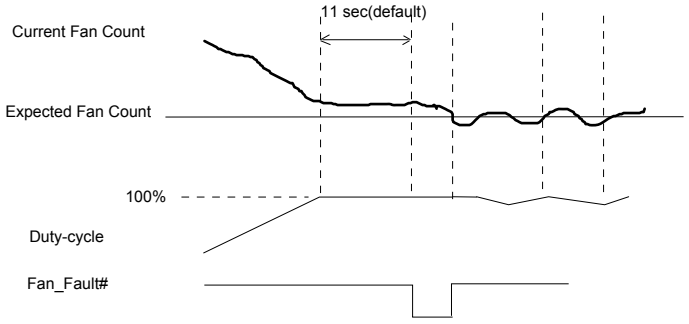


Figure 12 FAN_FAULT# event

(2). After the period of detecting fan full speed, PWM_Duty > Min. Duty, fan count is still in 0xFFF.

5.3 ACPI Function

The Advanced Configuration and Power Interface (ACPI) is a system for controlling the use of power in a computer. It lets computer manufacturer and user to determine the computer's power usage dynamically.

There are three ACPI states that are of primary concern to the system designer and they are designated S0, S3 and S5. S0 is a full-power state; the computer is being actively used in this state. The other two are called sleep states and reflect different power consumption when power-down. S3 is a state that the processor is powered down but the last procedural state is being stored in memory which is still active. S5 is a state that memory is off and the last procedural state of the processor has been stored to the hard disk. Take S3 and S5 as comparison, since memory is fast, the computer can quickly come back to full-power state, the disk is slower than the memory and the computer takes longer time to come back to full-power state. However, since the memory is off, S5 draws the minimal power comparing to S0 and S3.

It is anticipated that only the following state transitions may happen:

S0→S3, S0→S5, S5→S0, S3→S0 and S3→S5.

Among them, S3→S5 is illegal transition and won't be allowed by state machine. It is necessary to enter S0 first in order to get to S5 from S3. As for transition S5→S3 will occur only as an immediate state during state transition from S5→S0. It isn't allowed in the normal state transition.

The below diagram described the timing, the always on and always off, keep last state could be set in control register. In keep last state mode, one register will keep the status of before power loss. If it is power on before power loss, it will remain power on when power is resumed, otherwise, if it is power off before power loss, it will remain power off when power is resumed.

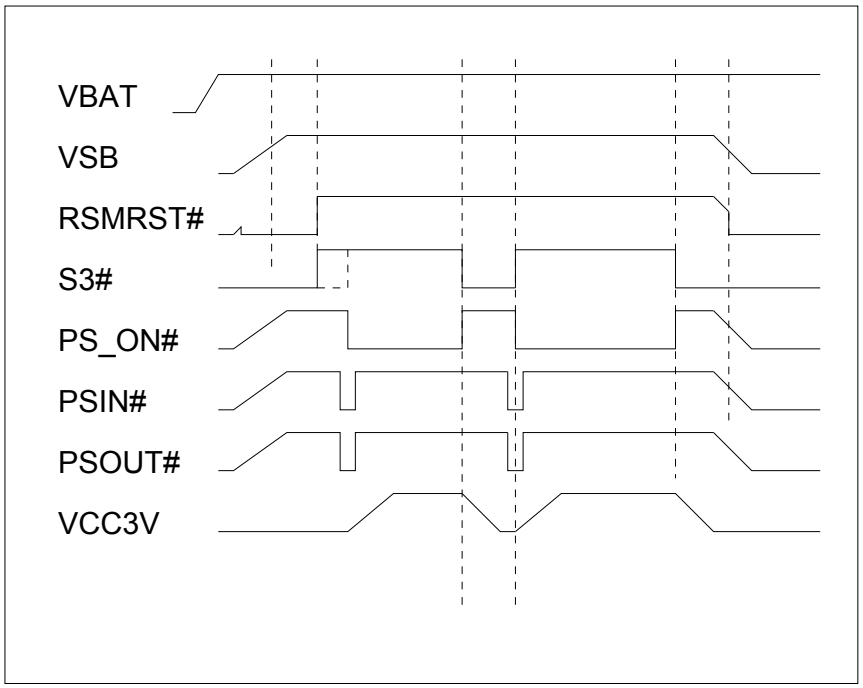


Figure 13 Default timing: Always off

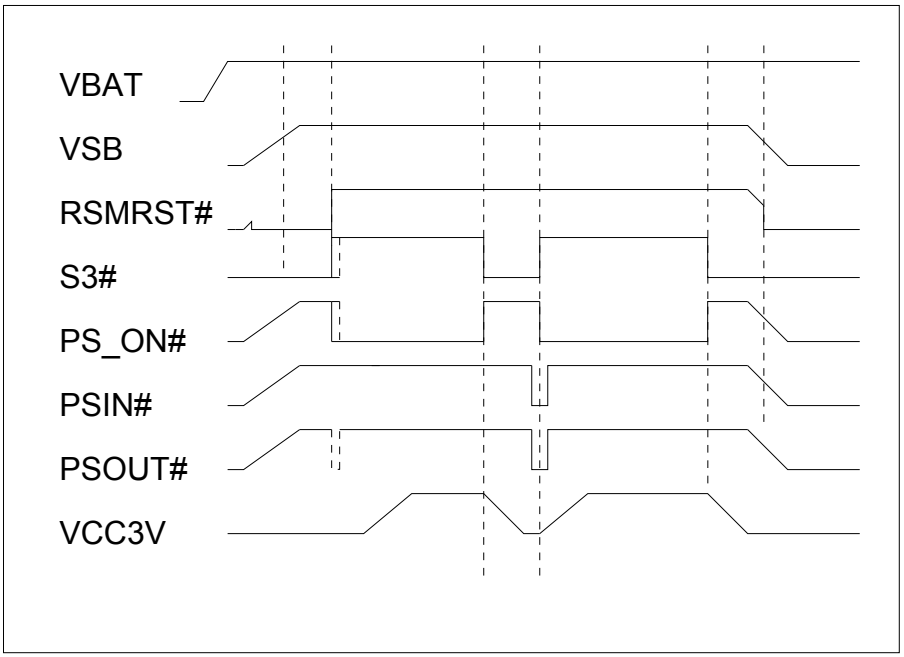
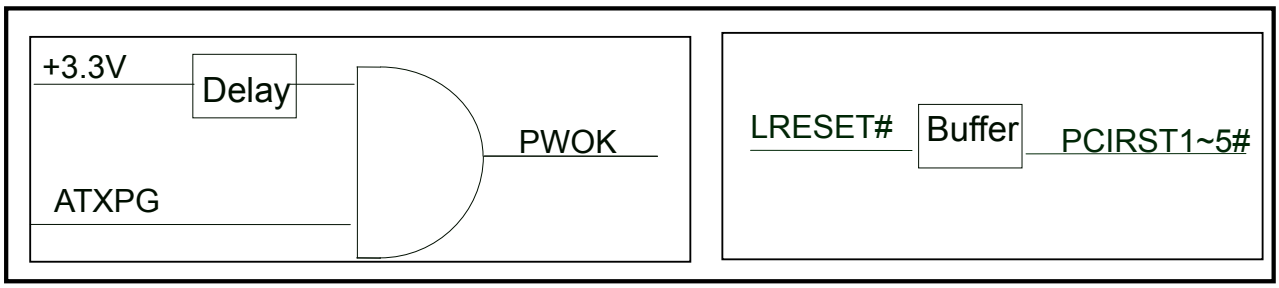


Figure 14 Optional timing: Always on

PCI Reset and PWOK Signals

The F71869A supports 5 output buffers for 5 reset signals.



So far as the PWOK issue is as the figure above. PWOK is delayed 400ms (default) as VCC arrives 2.8V, and the delay timing can be programmed by register. An additional delay could be added to PWOK (0ms, 100ms, 200ms and 400ms). If RSTCION# and PCIRST4#/PCIRST5# are enabled, RSTCON# could be programmed to be asserted via PWROK or PCIRST4#/PCIRST5#.

5.4 Power Timing Control Sequence

The F71869A offers 4 timing pins which are designed for AMD platform power sequence control including VDIMM, VDDA, Vcore, and VLDT (default) or other timing application purposes. All the timings on/off are relative to S3#/S5# and can be programmed by the register 0x0AF7. As shown in the below figure, the default timings of TIMING_1~4 are displayed in blue lines, and all the timings are enabled in the S0 state except TIMING_1. However, TIMING_2~4 can be programmed to enable in the S3 state, and TIMING_1 can also be programmed to disable in the S3 state, like the dotted blue line shown in the figure below.

VDDOK_D400 is the PWOK delay timing from VDD3VOK. The default setting is that delay 400ms, there are 100ms, 200ms, and 300ms for option. It can be set in the register 0x0AF5.

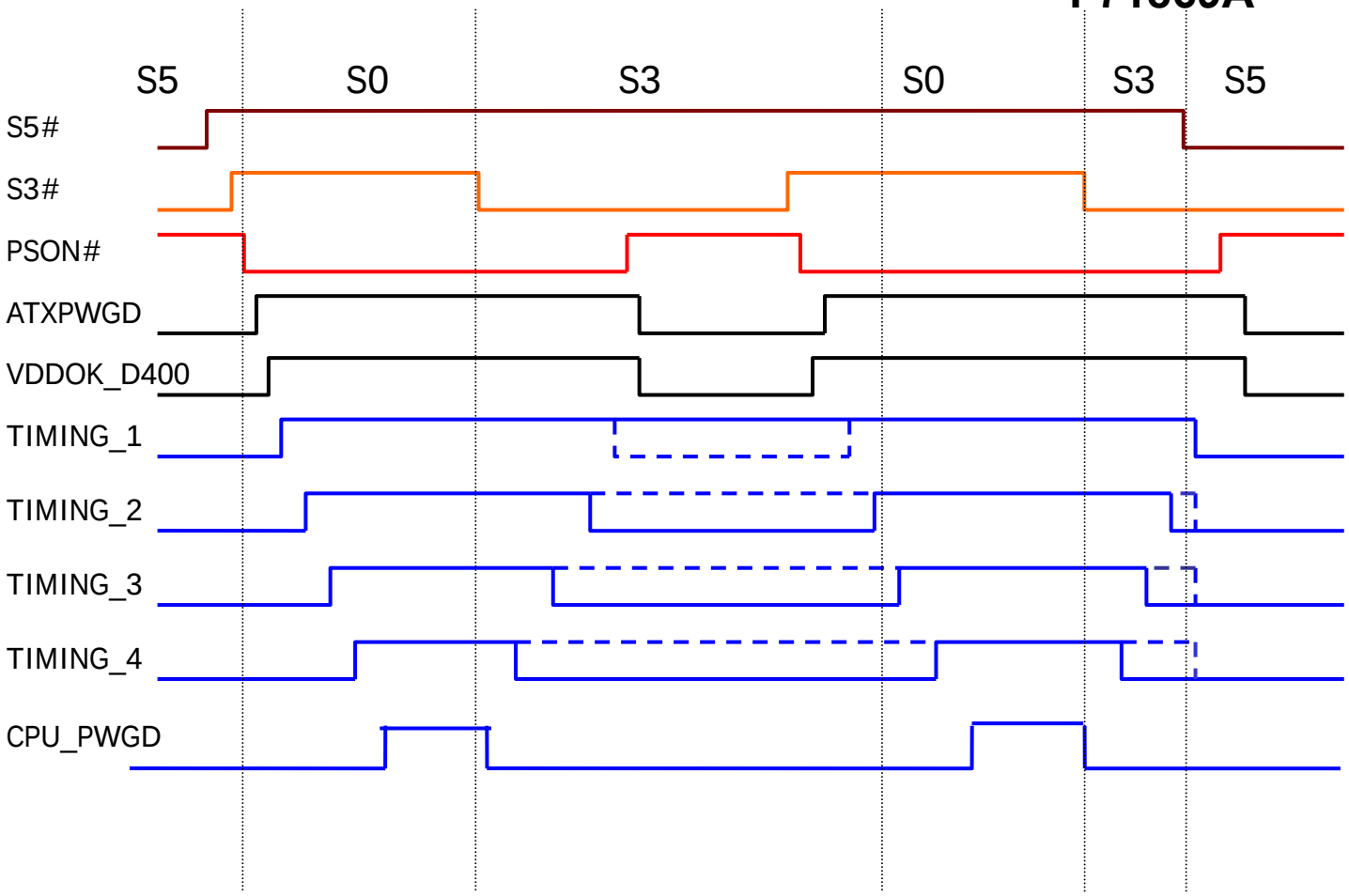


Figure 15 Timing on/off sequence

5.5 S_3_Gate#, S_{3P5}_Gate# and S_{0P5}_Gate# Timing

The F71869A provides three additional timing switching pins which are named as S_3_Gate#, S_{3P5}_Gate# and S_{0P5}_Gate#. They can be applied in the certain applications about power switch which depends on the ACPI states. The detail timing can be referred in the following diagrams. The default timing of S_{0P5}_Gate# in the S5 state is low, but it can be programmed high by the register 0x0AF6.

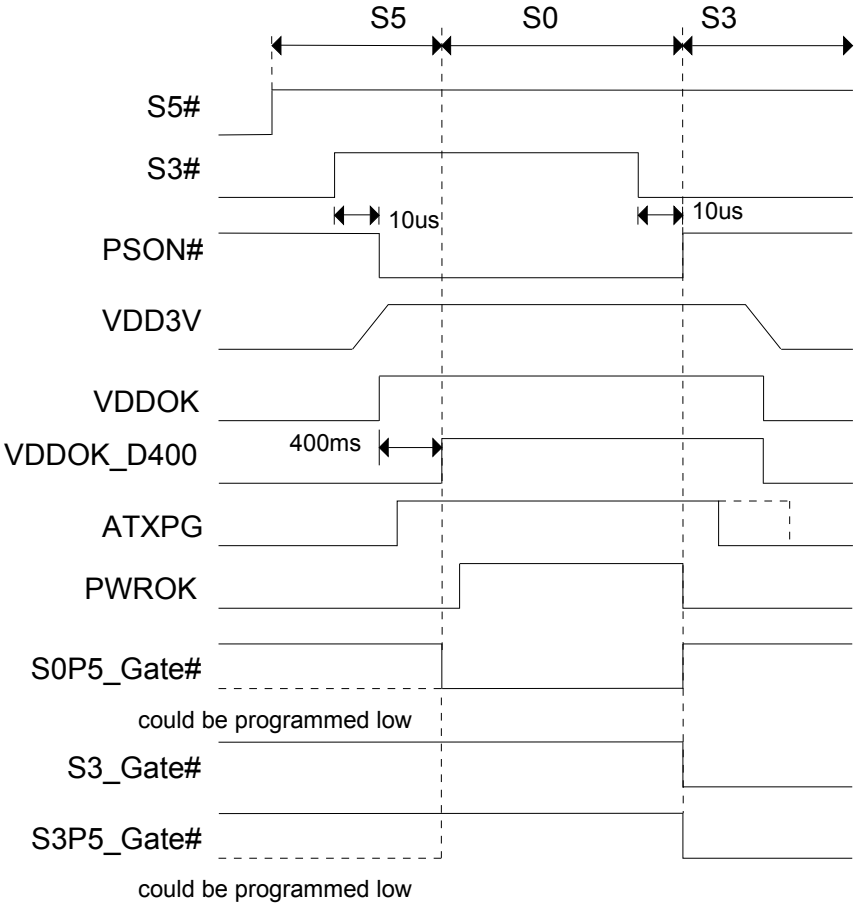


Figure 16 Timing chart of S5->S0->S3

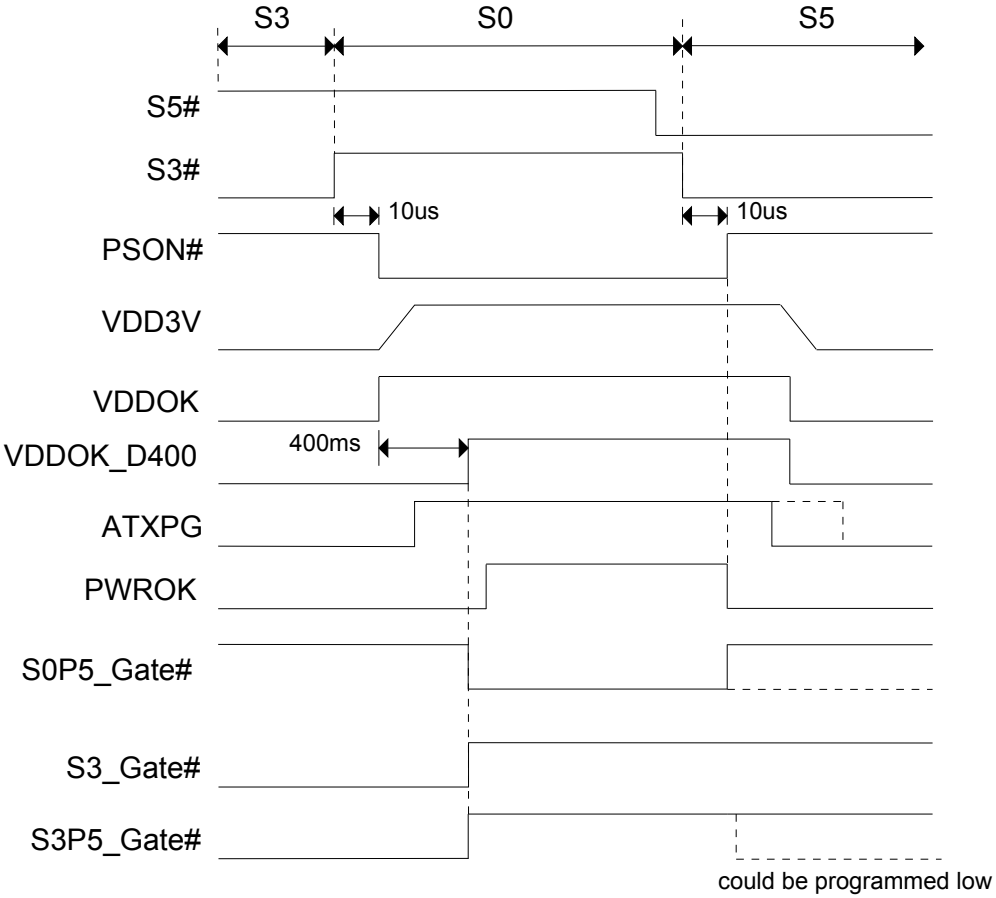


Figure 17 Timing chart of S3->S0->S5

5.6 AMD TSI and Intel PECI 3.0 Functions

The F71869A provides Intel PECI/AMD TSI interfaces for new generational CPU temperature sensing. In AMDSI interface, there are SIC and SID signals for temperature information reading from AMD CPU. The SIC signal is for clocking use, the other is for data transferring. More detail, please refer register description.

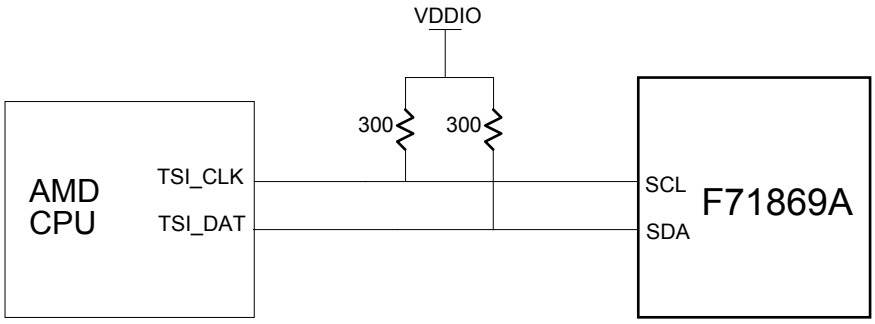


Figure 18 AMD TSI typical application

In Intel PECI interface, the F71869A can connect to CPU directly. The F71869A can read the temperature data from CPU, than the fan control machine of F71869A can implement the Fan to cool down CPU temperature. The application circuit is as below.

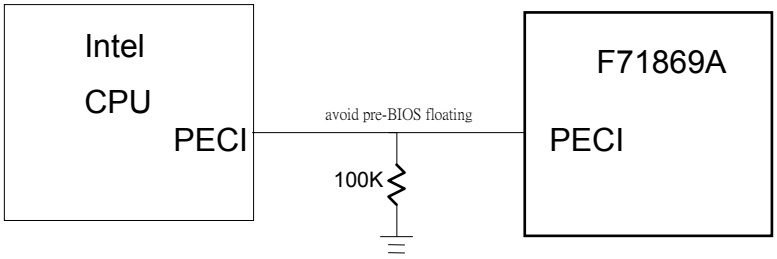


Figure 19 INTEL PECI Typical Application

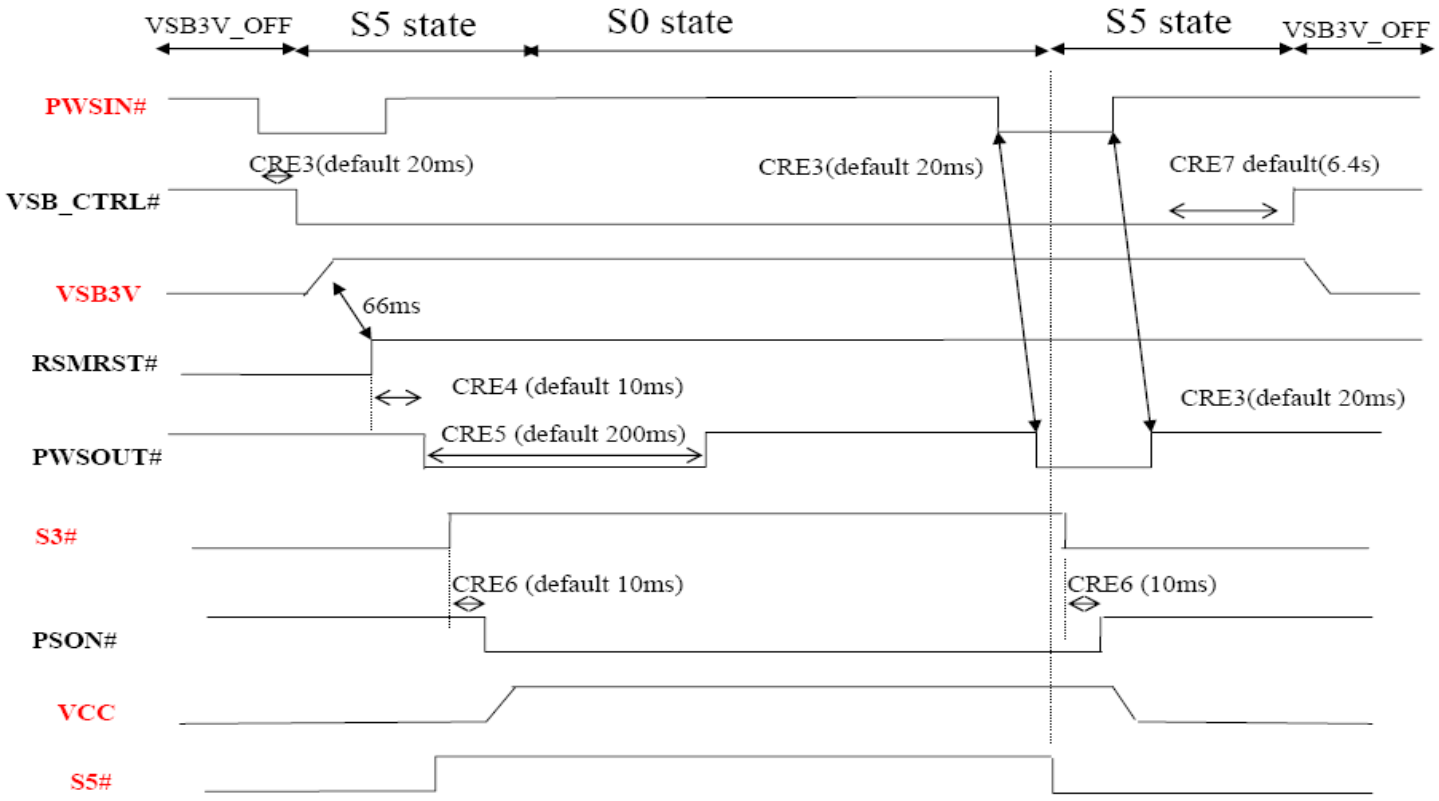
In Intel PECI 3.0 Spec., it's including below commands. The F71869A integrated most of those commands for future advantage application. More detail, please refer the register descriptions.

F71869A Support	PECI 3.0 Command Name	PECI 1.0 Command Name	Status
V	Ping( )	Ping( )	
V	GetTemp( )	GetTemp( )	
V	GetDIB( )		
V	RdIAMSR( )		
-	WrIAMSR( )		
-	RdPCIConfigLocal( )		Not Available in Mobile/DT
-	WrPCIConfigLocal( )		Not Available in Mobile/DT
-	RdPCIConfig( )		Not Available in Mobile/DT
-	WrPCIConfig( )		Not Available in Mobile/DT
V	RdPkgConfig( )		
V	WrPkgConfig( )		

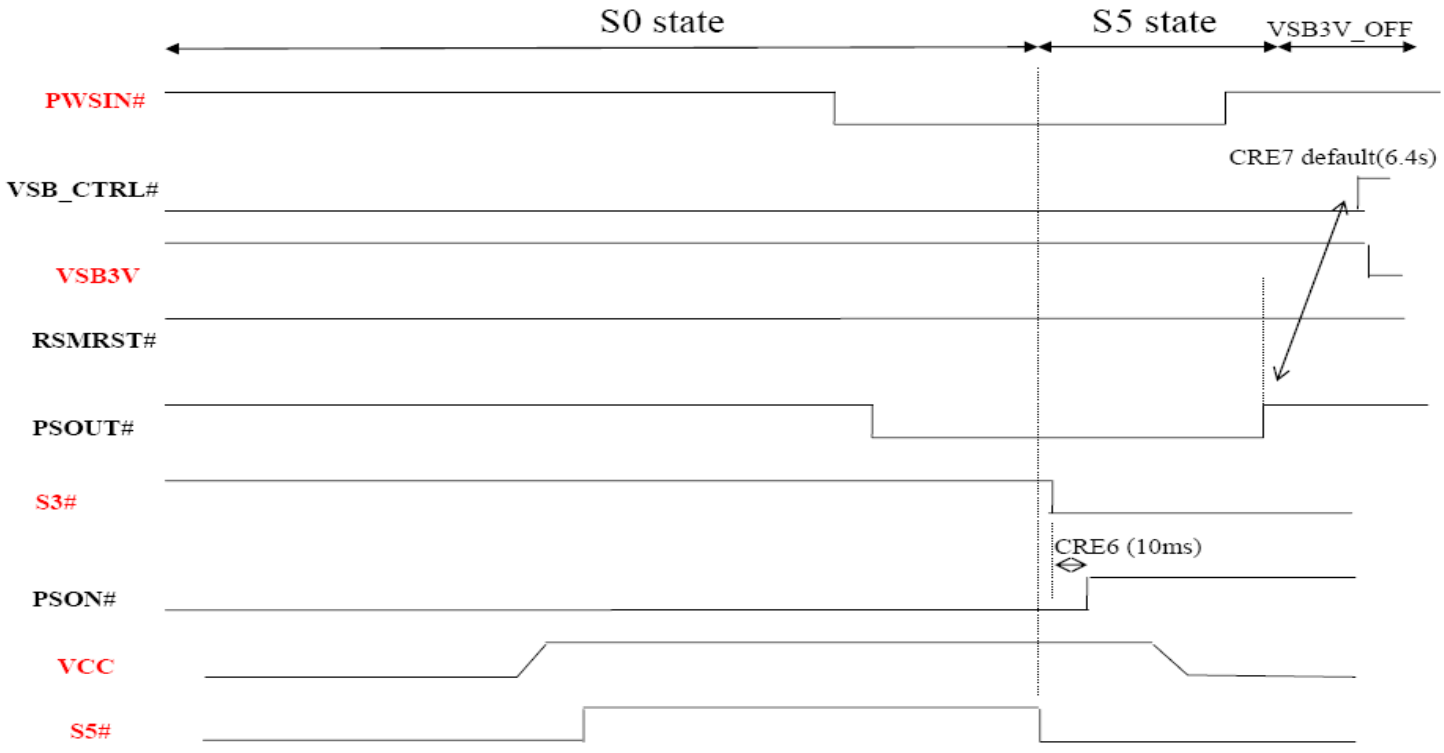
5.7 ErP Power Saving Function

The two pins, ERP_CTRL0# and ERP_CTRL1#, which control the standby power rail on/off to fulfill the purpose which decreases the power consumption when the system in the sleep state or the soft-off state. These two pins connected to the external PMOSs and the defaults are high in the sleep state in order to cut off all the standby power rails to save the power consumption. If the system needs to support wake-up function, the two pins can be programmable to set which power rail is turned on. The programmable register is powered by battery. So, the setting is kept even the AC power is lost when the register is set. At the power saving state (FINTEK calls it G3-like state), the F71869A consumes 5VSB power rail only to realize a low power consumption system. Below is ErP function's timing graphs.

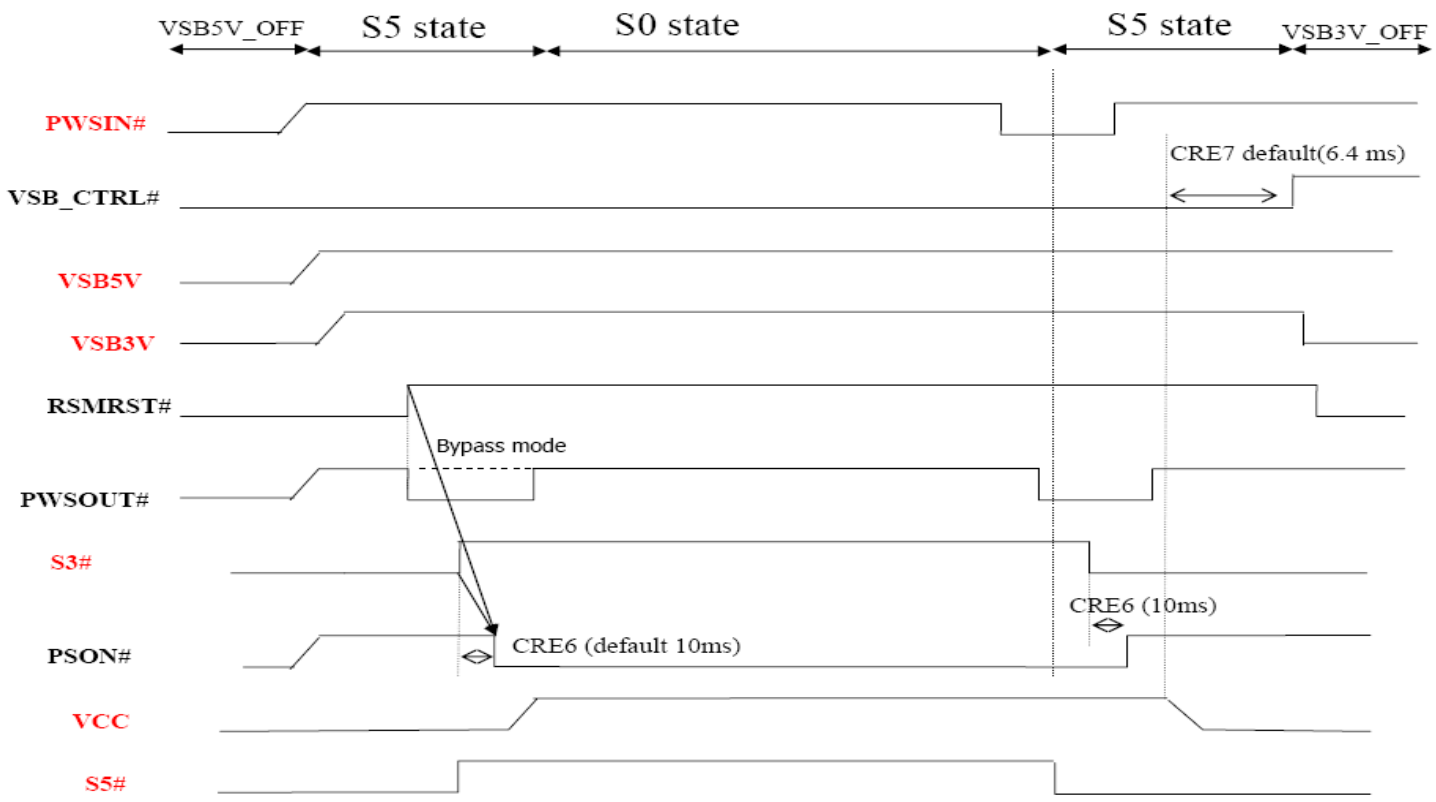
Boot From VSB3V OFF



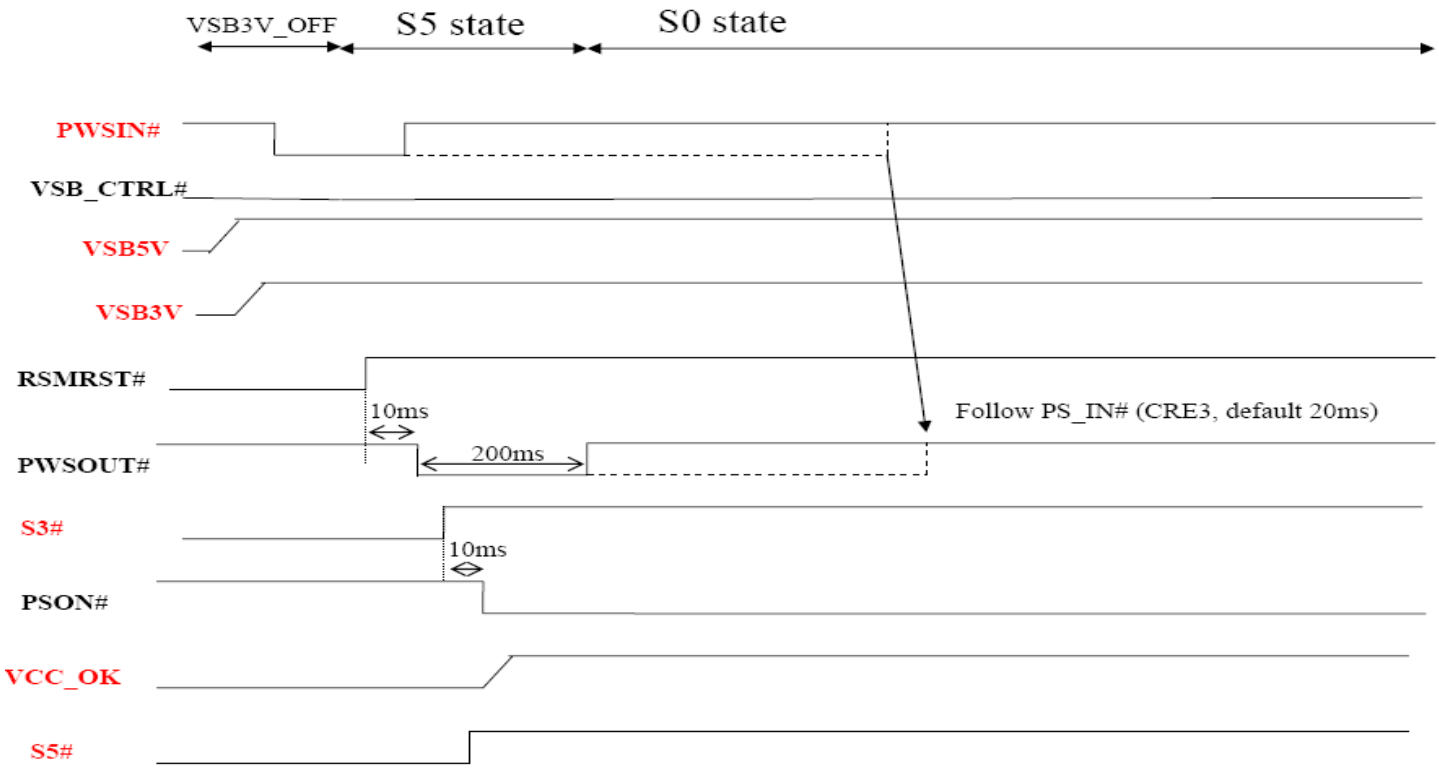
PSIN_IN# Gating VSB3V OFF



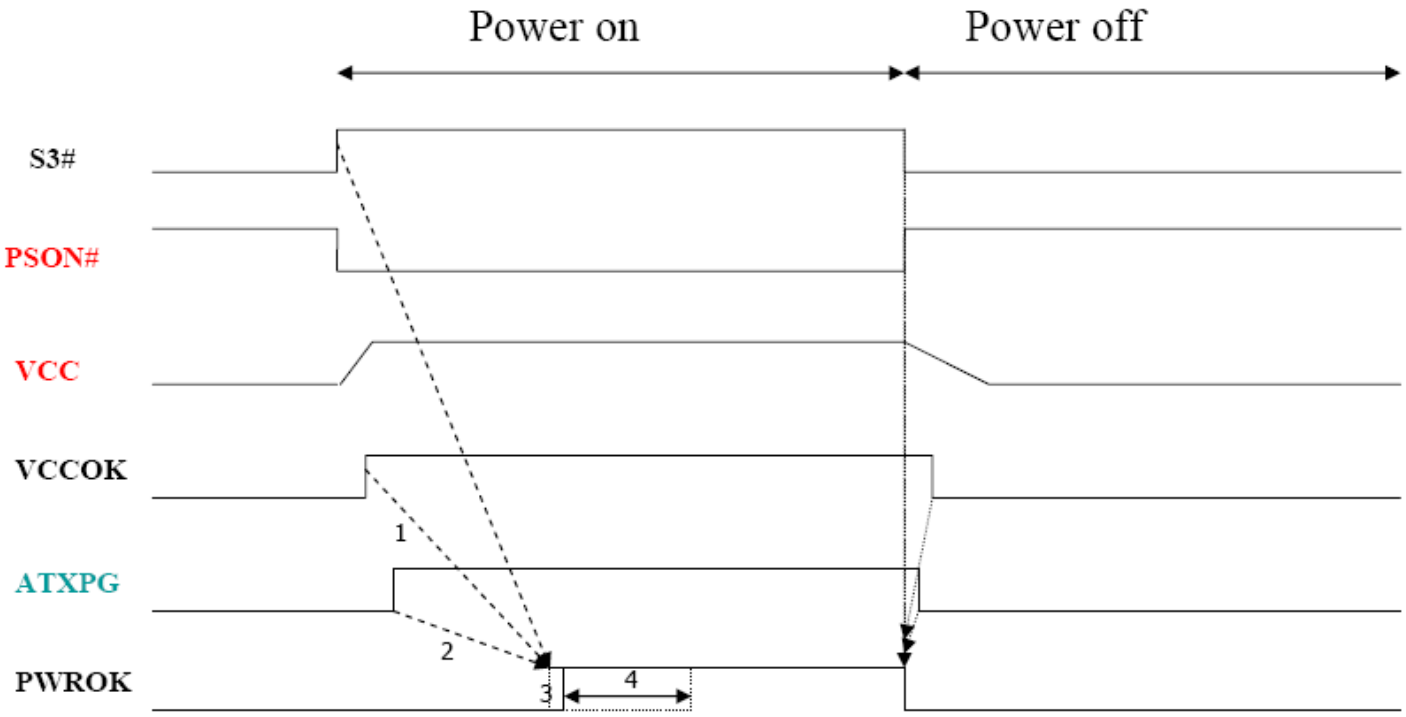
Boot From VSB5V AC lost & always on



Boot From VSB5V AC lost & always off



PWROK



1. VCCOK delay 100/200/300/400ms (default)
2. Delay 100~120ms
3. Delay 1ms
4. Extra delay: 0 (default) /100/200/400ms

5.8 CIR Function

The F71869A is compatible with Microsoft Windows Vista and Windows 7 IR Receiver or Transceiver Emulation Device which supports RC6 & QP protocol. It Supports 1 IR transceiver functions for blaster application and 1 IR receiver with long range frequency and another with wide band application. In power function, The F71869A supports Vista and Windows 7 wakeup programming function when the PC is in the S3 state. The F71869A decode IR protocol via the same Vista and Windows 7 wakeup programming key. The F71869A is asserted PME or PSOUT to wakeup PC system. Where wake up programming function is reference from Microsoft Vista and windows 7 remote controller specification.

The F71869A supports 1 IR transceiver function for blaster application and two IR receivers for long range frequency and wideband application. The wide-band receiver is necessary to support IR learning, IR-blasting and set-top box control.

The long-range receiver is a receiver which has the following characteristics:

1. Works at a distance of 10 meters.
2. Demodulates the signal inside the receiver part
3. Has a BPF which works with carriers from 32-60 kHz.

The wide-band receiver is a receiver part which has the following characters:

1. Works at a distance of approximately 5 centimeters.
2. Does not demodulate the signal inside the receiver part
3. Works with carriers from 32-60 kHz. (Probably doesn't have a BPF, but still has the same (or wider) range.

About IR information, reference Microsoft Windows Vista / 7 IR receiver or transceiver emulation device spec.

5.9 Intel Cougar Point Timing (CPT)

The F71869A supports Intel Cougar Point Chipset timing for Sandy Bridge. There are 4 pins for CPT control: SUS_WARN#, SUS_ACK#, SLP_SUS# and DPWROK.

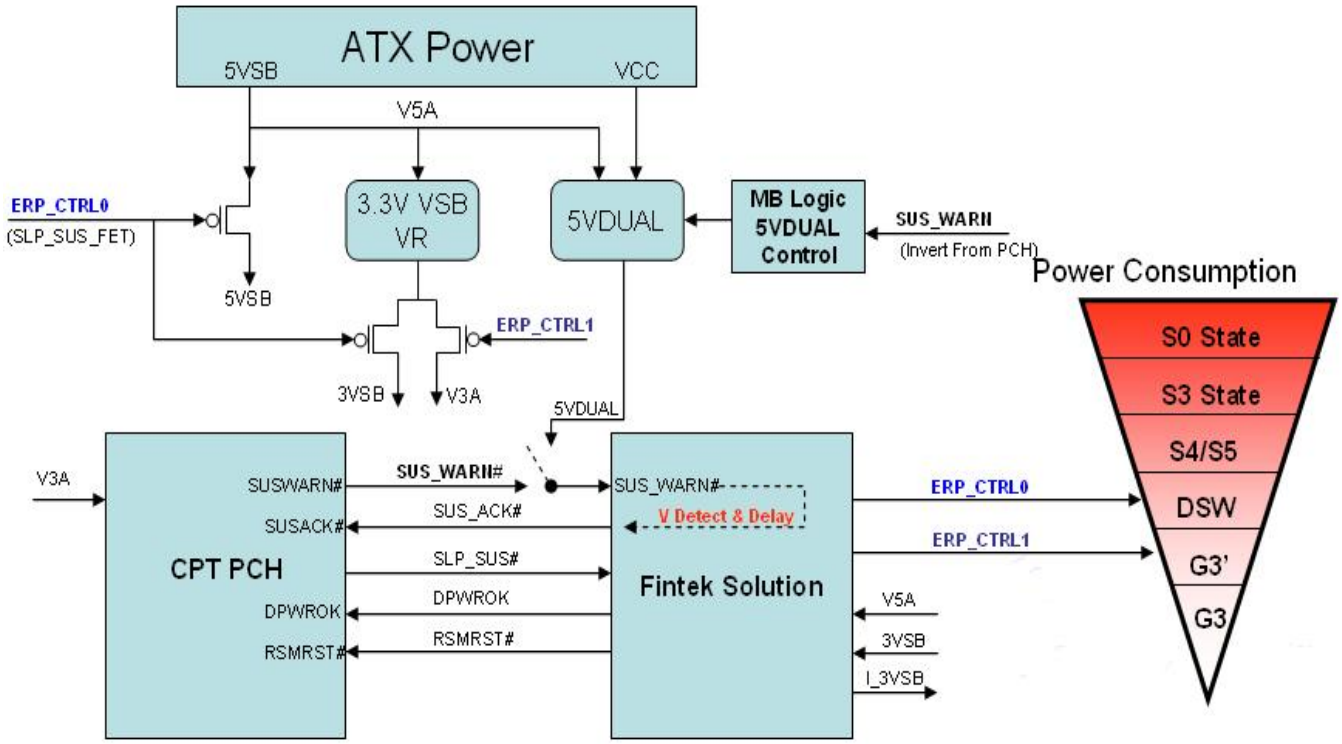
For entering Intel Deep Sleep Well (DSW) state, the PCH will assert SUS_WARN# and turn off 5VDUAL. After the level of 5VDUAL is lower than 1.05V, F71869A will assert SUS_ACK# to inform PCH it is ready for entering DSW. Finally, PCH will ramp down the internal VccSUS and assert SLP_SUS# to F71869A. F71869A will turn off the 5VSB and 3VSB by ERP_CTRL0# and enter the DSW state.

To exit DSW state, PCH will de-assert SLP_SUS#, turn on the SUS rail FETs and ramp up internal 1.05V VccSUS. After the SUS rails voltages are up, RSMRST# will be desserted and the PCH will release SUS_WARN# so that the 5VDUAL will ramp up.

Because the DSW function is controlled by F71869A instead of controlled by PCH directly, there will be more wakeup events such as LAN, KB/Mouse, SIO RI# wake up rather than the 3 wakeup events (RTC, Power Button and GPIO27) for Intel DSW.

In order to achieve lower power consumption, F71869A provides the ERP_CTRL1# to turn off the V3A so that the system can enter the Fintek G3' state.

The block diagram below shows how the connection and control method for F71869A and PCH.

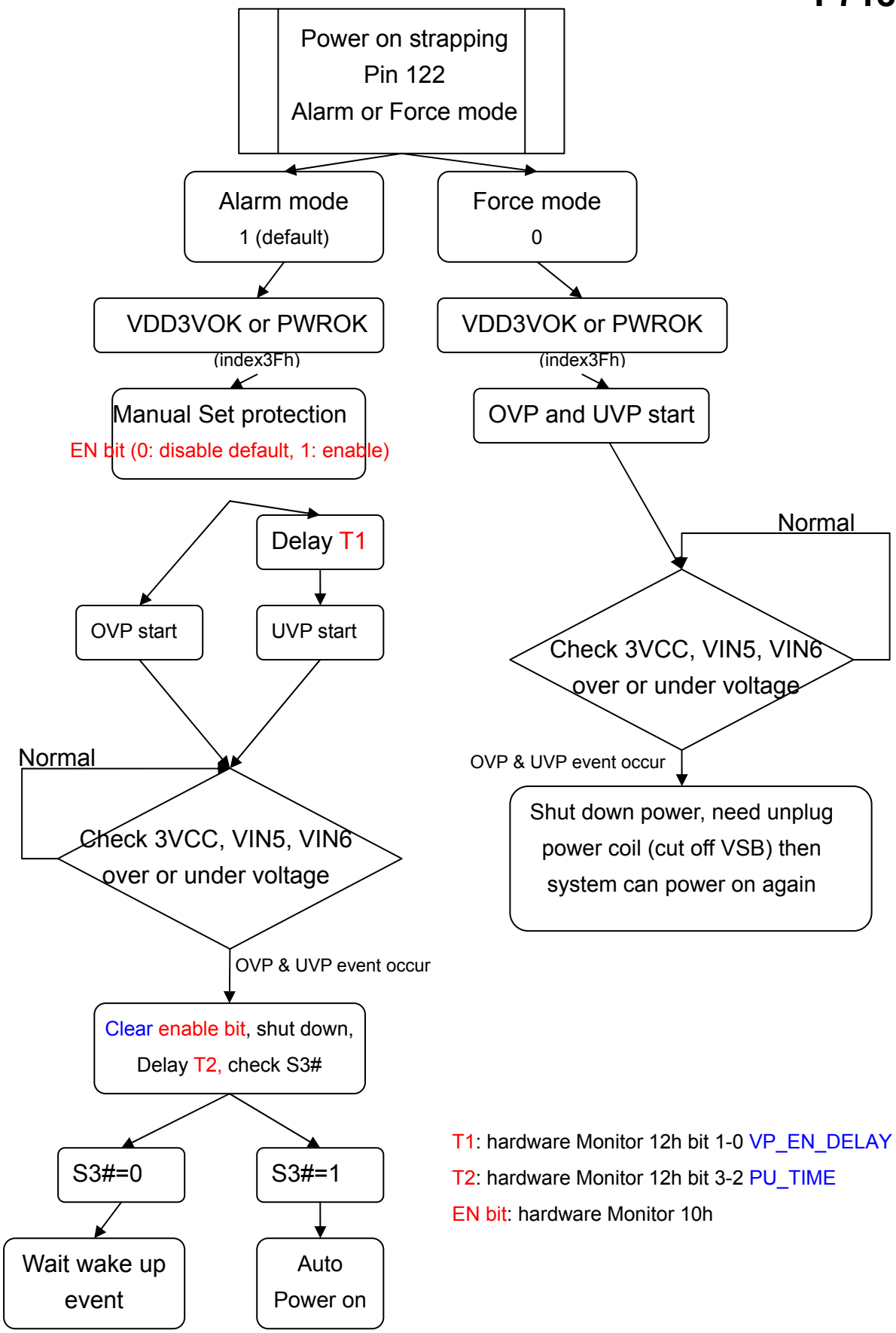


5.10 Scan Code Function

F71869A has 5 GPIO pins (GPIO 50 to GPIO 54) support scan code. These pins can not only be set to volume up/down, mute and PWM up/down but also any function keys on keyboard. Because the protocol for these 5 pins is scan code, so we don't need a driver to connect this function to OS. If the button for the GPIO has been pressed continuesly over nearly 1 second (delay time), the GPIO will repeatedly sending this function in an interval of 50 ms (repeat time). The delay time could be set from 0.5 to 1.5 sec. The repeat time could be set from 50, 100, 250 to 500 ms.

5.11 Over Voltage Protection

F71869A anti surge protection function could protect the damage from voltage spikes via over voltage & under voltage protection (OVP & UVP) function. Hardware strapping pin 122 default is disabled alarm mode. Voltage protection function is enabled via setting the related register. When force mode occurs, the system would shut down and then can not boot at all. Only re-plugging the power code (cut off VSB) could re-activate or re-boot the system at the force mode. Please see below table for detail information:



T1: hardware Monitor 12h bit 1-0 VP_EN_DELAY

T2: hardware Monitor 12h bit 3-2 PU_TIME

EN bit: hardware Monitor 10h

6. Register Description

The configuration register is used to control the behavior of the corresponding devices. To configure the register, using the index port to select the index and then writing data port to alter the parameters. The default index port and data port are 0x4E and 0x4F respectively. Pull down the SOUT1 pin to change the default value to 0x2E/0x2F. To enable configuration, the entry key 0x87 must be written to the index port. To disable configuration, write exit key 0xAA to the index port. Following is a example to enable configuration and disable configuration by using debug.

-o 4e 87
-o 4e 87 (enable configuration)
-o 4e aa (disable configuration)

The Following is a register map (total devices) grouped in hexadecimal address order, which shows a summary of all registers and their default value. Please refer each device chapter if you want more detail information.

Global Control Registers

"-" Reserved or Tri-State

Global Control Registers									
Register 0x[HEX]	Register Name	Default Value MSB							LSB
02	Software Reset Register	-	-	-	-	-	-	-	0
07	Logic Device Number Register (LDN)	0	0	0	0	0	0	0	0
20	Chip ID Register 1	0	0	0	1	0	0	0	0
21	Chip ID Register 2	0	0	0	0	0	1	1	1
23	Vendor ID Register 1	0	0	0	1	1	0	0	1
24	Vendor ID Register 2	0	0	1	1	0	1	0	0
25	Software Power Down Register	-	-	-	-	0	0	0	0

26	UART IRQ Sharing Register	0	-	0	-	-	0	0	0
27	Configuration Port Select Register	1/0	0	1/0	1/0	-	-	-	1/0
28	Multi-function Select Register1	0	0	1	1	1	0	0	0
29	Multi-function Select Register2	0	1	1	0	1	1	1	1
2A	Multi-function Select Register3	0	0	0	0	1	1	1	1
2B	Multi-function Select Register4	0	0	0	0	1	1	1	1
2C	Multi-function Select Register 5	0	0	0	0	0	0	0	0
2D	Wakeup Control Register	0	0	1	0	1	0	0	0

Device Configuration Registers

"-" Reserved or Tri-State

FDC Device Configuration Registers (LDN CR00)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	FDC Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	1	1	1	1	0	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	1	0
74	DMA Channel Select Register	-	-	-	-	-	0	1	0
F0	FDD Mode Register	0	-	-	0	1	1	1	0
F2	FDD Drive Type Register	-	-	-	-	-	-	1	1
F4	FDD Selection Register	-	-	-	0	0	-	0	0
UART1 Device Configuration Registers (LDN CR01)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	UART1 Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	1	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	0	0
F0	RS485 Enable Register	-	-	0	0	-	-	-	-
UART2 Device Configuration Registers (LDN CR02)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	UART2 Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	1	1	1	1	0	0	0

70	IRQ Channel Select Register	-	-	-	-	0	0	1	1
F0	RS485 Enable Register	-	-	-	0	0	0	-	-
F1	SIR Mode Control Register	-	-	0	0	0	1	0	0

Parallel Port Device Configuration Registers (LDN CR03)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Parallel Port Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	0	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	1	1
74	DMA Channel Select Register	-	-	-	0	-	0	1	1
F0	PRT Mode Select Register	0	1	0	0	0	0	1	0

Hardware Monitor Device Configuration Registers (LDN CR04)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	H/W Monitor Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	0	0	1	0	1	0	1
70	IRQ Channel Select Register	-	-	-	-	0	0	0	0

KBC Device Configuration Registers (LDN CR05)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	KBC Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	1	1	0	0	0	0	0
70	KB IRQ Channel Select Register	-	-	-	-	0	0	0	1
72	Mouse IRQ Channel Select Register	-	-	-	-	1	1	0	0
F0	Clock Select Register	1	0	-	-	-	-	1	1
FE	Swap Register	1	-	-	0	0	0	0	1
FF	User Wakeup Code Register	0	0	1	0	1	0	0	1

GPIO Device Configuration Registers (LDN CR06)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	GPIO Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
70	GPIRQ Channel Select Register	-	-	-	-	0	0	0	0

F0	GPIO Output Enable Register	-	-	0	0	0	0	0	0
F1	GPIO Output Data Register	-	-	1	1	1	1	1	1
F2	GPIO Pin Status Register	-	-	-	-	-	-	-	-
F3	GPIO Drive Enable Register	-	-	0	0	0	0	0	0
E0	GPIO1 Output Enable Register	0	0	0	0	0	0	0	0
E1	GPIO1 Output Data Register	1	1	1	1	1	1	1	1
E2	GPIO1 Pin Status Register	-	-	-	-	-	-	-	-
E3	GPIO1 Drive Enable Register	0	0	0	0	0	0	0	0
E4	GPIO1 PME Enable Register	0	0	0	0	0	0	0	0
E5	GPIO1 Detect Edge Select Register	0	0	0	0	0	0	0	0
E6	GPIO1 PME Status Register	0	0	0	0	0	0	0	0
D0	GPIO2 Output Enable Register	0	0	0	0	0	0	0	0
D1	GPIO2 Output Data Register	1	1	1	1	1	1	1	1
D2	GPIO2 Pin Status Register	-	-	-	-	-	-	-	-
D3	GPIO2 Drive Enable Register	0	0	0	0	0	0	0	0
C0	GPIO3 Output Enable Register	0	0	0	0	0	0	0	0
C1	GPIO3 Output Data Register	1	1	1	1	1	1	1	1
C2	GPIO3 Pin Status Register	-	-	-	-	-	-	-	-
B0	GPIO4 Output Enable Register	-	-	-	-	0	0	0	0
B1	GPIO4 Output Data Register	-	-	-	-	1	1	1	1
B2	GPIO4 Pin Status Register	-	-	-	-	-	-	-	-
B3	GPIO4 Drive Enable Register	-	-	-	-	0	0	0	0
B4	GPIO4 PME Enable Register	-	-	-	-	0	0	0	0
B5	GPIO4 Detect Edge Select Register	-	-	-	-	0	0	0	0
B6	GPIO4 PME Status Register	-	-	-	-	0	0	0	0
A0	GPIO5 Output Enable Register	-	-	-	0	0	0	0	0
A1	GPIO5 Output Data Register	-	-	-	1	1	1	1	1
A2	GPIO5 Pin Status Register	-	-	-	-	-	-	-	-
A4	GPIO5 PME Enable Register	-	-	-	0	0	0	0	0
A5	GPIO5 Detect Edge Select Register	-	-	-	0	0	0	0	0
A6	GPIO5 PME Status Register	-	-	-	0	0	0	0	0
A9	GPIO5 KBC Emulation Control Register 1	0	0	0	0	0	0	0	0
AB	GPIO5 KBC Emulation Make Code Register	0	0	0	0	0	0	0	0
AC	GPIO5 KBC Emulation Prefix Code Register	1	1	1	0	0	0	0	0
AD	GPIO5 KBC Emulation Status Register 1	0	0	0	0	0	0	0	0
AE	GPIO5 KBC Emulation Status Register 2	0	0	0	0	0	0	0	0
AF	GPIO5 KBC Emulation Control Register 2	0	1	0	0	0	0	0	0

90	GPIO6 Output Enable Register	0	0	0	0	0	0	0	0
91	GPIO6 Output Data Register	1	1	1	1	1	1	1	1
92	GPIO6 Pin Status Register	-	-	-	-	-	-	-	-
80	GPIO7 Output Enable Register	0	0	0	0	0	0	0	0
81	GPIO7 Output Data Register	1	1	1	1	1	1	1	1
82	GPIO7 Pin Status Register	-	-	-	-	-	-	-	-
83	GPIO7 Drive Enable Register	0	0	0	0	0	0	0	0

WDT Device Configuration Registers (LDN CR07)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
F0	Watchdog Timer Enable Register	-	-	-	-	-	-	-	1
F2	BUS Manual Register	0	0	0	0	0	0	0	0
F3	Key Data Register	0	0	0	0	0	0	0	0
F4	BUSIN Status Register	-	-	-	-	-	-	-	-
F5	WDT Unit Select Register	-	0	-	0	0	0	0	0
F6	WDT Count Register	0	0	0	0	1	0	1	0
F7	Watchdog Timer PME Register	0	0	0	-	-	-	-	0

CIR Configuration Register (LDN CR08)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	CIR Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
70	CIR IRQ Channel Select Register	-	-	-	-	0	0	0	0
F0	Reserved	-	-	-	-	-	-	-	-
F1	Reserved	-	-	-	-	-	-	-	-
F8	Reserved	0	0	0	0	0	0	0	0
F9	Reserved	0	0	0	0	0	0	0	0
FA	Reserved	1	0	0	0	0	0	0	0
FB	Reserved	0	0	1	1	1	0	1	1
FC	Reserved	0	0	0	0	0	0	0	0
FD	Reserved	0	0	0	0	0	0	0	0
FE	Reserved	0	0	0	0	0	0	0	0

PME, ACPI, and ERP Power Saving Device Configuration Registers (LDN CR0A)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	PME Device Enable Register	-	-	-	-	-	-	-	0

E0	ERP Enable Register	0	-	-	-	-	-	0	0
E1	ERP Control Register	1	1	0	0	1	1	0	0
E2	ERP Control Register	-	0	1	1	1	1	0	-
E3	ERP PSIN Deb-Register	0	0	0	1	0	0	1	1
E4	ERP RSMRST Deb-Register	0	0	0	0	1	0	0	1
E5	ERP PSOUT Deb-Register	1	1	0	0	0	1	1	1
E6	ERP PSON Deb-Register	0	0	0	0	1	0	0	1
E7	ERP S5 Delay Register	0	1	1	0	0	0	1	1
E8	Wakeup Enable Register	0	-	0	0	1	0	0	0
E9	ERP S3 Delay Register	0	0	0	0	1	1	1	1
EC	ERP Mode Select Register	0	0	0	-	-	-	-	-
ED	ERP WDT Control Register	-	-	-	-	-	-	0	0
EE	ERP WDT Timer	-	-	-	-	-	-	-	0
F0	PME Event Enable Register 1	0	0	0	0	0	0	0	0
F1	PME Event Status Register 1	-	-	-	-	-	-	-	-
F2	PME Event Enable Register 2	-	-	-	0	-	0	0	0
F3	PME Event Status Register 2	-	-	-	-	-	-	-	-
F4	Keep Last State Select Register	0	0	0	0	0	1	1	0
F5	VDDOK Delay Select Register	0	0	0	1	1	1	0	0
F6	PCIRST Control Register	0	0	0	1	1	1	1	1
F7	Power Sequence Control Register	1	0	0	0	0	1	1	0
F8	LED VCC Control Register	0	0	0	0	0	0	0	0
F9	LED VSB Control Register	-	0	0	0	0	0	0	0
FA	LED VSB Additional Control Register	-	0	0	0	-	0	0	0
FC	Intel DSW Delay Register	-	-	-	-	0	1	1	1
FE	RI De-bounce Select Register	0	0	-	0	-	-	0	0

6.1 Global Control Registers

6.1.1 Software Reset Register — Index 02h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	SOFT_RST	R/W	0	Write 1 to reset the register and device powered by VDD (3VCC).

6.1.2 Logic Device Number Register (LDN) — Index 07h

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Select FDC device configuration registers. 01h: Select UART 1 device configuration registers. 02h: Select UART 2 device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select WDT device configuration registers. 0ah: Select PME & ACPI device configuration registers.

6.1.3 Chip ID Register 1 — Index 20h

Bit	Name	R/W	Default	Description
7-0	Chip_ID1	R	10h	Chip ID1

6.1.4 Chip ID Register 2 — Index 21h

Bit	Name	R/W	Default	Description
7-0	Chip_ID2	R	07h	Chip ID2

6.1.5 Vendor ID Register 1 — Index 23h

Bit	Name	R/W	Default	Description
7-0	Vendor_ID1	R	19h	Vendor ID1

6.1.6 Vendor ID Register 2 — Index 24h

Bit	Name	R/W	Default	Description
7-0	Vendor_ID2	R	34h	Vendor ID2

6.1.7 Software Power Down Register — Index 25h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3	SOFTPD_PRT	R/W	0	Set “1” to power down Parallel Port. The clock will stop.
2	SOFTPD_UR2	R/W	0	Set “1” to power down UART 2. The clock will stop.

1	SOFTPD_UR1	R/W	0	Set “1” to power down UART 1. The clock will stop.
0	SOFTPD_FDC	R/W	0	Set “1” to power down FDC. The clock will stop.

6.1.8 UART IRQ Sharing Register — Index 26h

Bit	Name	R/W	Default	Description
7	CLK24M_SEL	R/W	0	0: CLKIN is 48MHz 1: CLKIN is 24MHz
6	Reserved	-	-	Reserved.
5	DPORT_DEC_SEL	R/W	0	0: The debug port address is 0x80. 1: The debug port address is UART2 base address.
4-3	Reserved	-	-	Reserved.
2	TX_DEL_1BIT	R/W	0	0: UART transmits data immediately after writing THR. 1: UART transmits data delay one bit time after writing THR.
1	IRQ_MODE	R/W	0	0: PCI IRQ sharing mode (low level). 1: ISA IRQ sharing mode (low pulse).
0	IRQ_SHAR	R/W	0	0: disable IRQ sharing of two UART devices. 1: enable IRQ sharing of two UART devices.

6.1.9 Configuration Port Select Register — Index 27h

Bit	Name	R/W	Default	Description
7	OVP_MODE	R/W	-	1: Alarm mode. Voltage protection is default disabled. 0: Force mode. Voltage protection is default enabled. This bit is power on strapped by RTS1#/STRAP_PROTECT. Pull down to select force mode.
6	TEMP_OUT_EN	R/W	0	Debug port output select. 0: 80 port data. 1: Temperature fetched by hardware mmonitor.
5	DPORT_EN	R/W	-	0: Disable debug port. 1: Enable debug port. This bit is power on strapped by GPIO26/SOUT2/SEGB/STRAP_DPORT. Pull down to disable.

4	PORT_4E_EN	R/W	-	0: The configuration register port is 2E/2F. 1: The configuration register port is 4E/4F. This register is power on trapped by SOUT1/ Config4E_2E. Pull down to select port 2E/2F.
3-1	Reserved	-	-	Reserved.
0	TIMING_EN	R	-	This bit is the pin status of TIMING_GPIO pin. 0: Disable power sequence control. 1: Enable power sequence control.

6.1.10 Multi-Function Select Register 1— Index 28h (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	FDC_GP_RST_SEL	R/W	0	Select GPIO5/GPIO3 reset signal. 0: Reset by LRESET#. 1: Reset by internal VSB3V power good.
6	Reserved	R/W	0	Reserved
5	PWR_ S3_Gate#_EN	R/W	1	0: S3_Gate#/GPIO05/WDTRST# functions as GPIO05/WDTRST# determined by GPIO05_EN. 1: S3_Gate#/GPIO05/WDTRST# functions as S3_Gate#.
4	PWR_ S3P5_Gate#_EN	R/W	1	0: S3P5_Gate#/SLOTOCC#/GPIO04 functions as SLOTOCC#/GPIO04 determined by GPIO04_EN. 1: S3P5_Gate#/SLOTOCC#/GPIO04 functions as S3P5_Gate#.
3	GPIO05_EN	R/W	1	0: S3_Gate#/GPIO05/WDTRST# functions as WDTRST if PWR_ S3_Gate#_EN is not set. 1: S3_Gate#/GPIO05/WDTRST# functions as GPIO05 is PWR_ S3_Gate#_EN is not set.
2	GPIO04_EN	R/W	0	0: S3P5_Gate#/SLOTOCC#/GPIO04 functions as SLOTOCC# if PWR_ S3P5_Gate#_EN is not set. 1: S3P5_Gate#/SLOTOCC#/GPIO04 functions as GPIO04 if PWR_ S3P5_Gate#_EN is not set.
1-0	Reserved	R/W	0	Reserved

6.1.11 Multi-Function Select Register 2 — Index 29h (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	GPIO17_EN	R/W	0	CPU_PWGD/GPIO17 function select. 0: The pin function is CPU_PWGD. 1: The pin function is GPIO17.
6	GPIO16_EN*	R/W	1	GPIO16/LED_VCC function select. 0: The pin function is LED_VCC. 1: The pin function is GPIO16. This bit is powered by VBAT.
5	GPIO15_EN	R/W	1	GPIO15/LED_VSB/ALERT# function select. {LED_VSB_EN, GPIO15_EN} 1x: The pin function is LED_VSB. 01: The pin function is GPIO15. 00: The pin function is ALERT#.
4	GPIO14_EN	R/W	0	WDTRST#/GPIO14 function select. 0: The pin function is WDTRST#. 1: The pin function is GPIO14.
3	GPIO13_EN	R/W	1	S_0P_5_Gate#/GPIO13/BEEP function select. If S_0P_5_Gate#_EN is set , the ping function is S_0P_5_Gate#, The pin function is determined by { S_0P_5_Gate#_EN, GPIO13_EN} 1x: The pin function is S_0P_5_Gate#. 01: The pin function is GPIO13. 00: The pin function is BEEP.
2	GPIO12_EN	R/W	1	GPIO12/ RSTCON#/FANCTL1 function select. 0: The pin function is FANCTL1. 1: The pin function is GPIO12.
1	GPIO11_EN	R/W	1	GPIO11/PCIRST5#/SDA function select. If IBX_ALT_EN is set , the ping function is SDA, otherwise the pin function is determined by this bit: 0: The pin function is PCIRST5#. 1: The pin function is GPIO11.

0	GPIO10_EN	R/W	1	GPIO10/PCIRST4#/SCL function select. If IBX_ALT_EN is set , the ping function is SCL, otherwise the pin function is determined by this bit: 0: The pin function is PCIRST4#. 1: The pin function is GPIO10.

6.1.12 Multi-Function Select Register 3 — Index 2Ah (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	LPT_GP_EN	R/W	0	Parallel Port/GPIO function select. 0: Pin 100 ~ 116 functions as Parallel Port. 1: Pin 100 ~ 116 functions as GPIO6 and GPIO7.
6	IBX_ALT_EN	R/W	0	Alternative IBX pin enable. 0: Disable IBX alternative pins. 1: Enable IBS alternative pins. See GPIO11_EN and GPIO10_EN for detail.
5	LED_VSB_EN	R/W	0	GPIO15/LED_VSB/ALERT# function select. {LED_VSB_EN, GPIO15_EN} 1x: The pin function is LED_VSB. 01: The pin function is GPIO15. 00: The pin function is ALERT#.
4	RSTCON_PIN_EN	R/W	0	RSTCON# Enable Register: 0: The pin function of GPIO12/ RSTCON#/FANCTL1 is GPIO12/ FANCTL1 1: The pin function of GPIO12/RSTCON#/FANCTL1 is RSTCON#.
3	S0P5_Gate# _EN	R/W	1	S0P5_Gate#/GPIO13/BEEP function select. If S0P5_Gate#_EN is set , the ping function is S0P5_Gate#, The pin function is determined by { S0P5_Gate#_EN, GPIO13_EN} 1x: The pin function is S0P5_Gate#. 01: The pin function is GPIO13. 00: The pin function is BEEP.
2	FDC_GP_EN	R/W	1	Set “1” will disable FDC and change the FDC pins to GPIOs.
1	UR2_GP_EN2	R/W	1	Set “1” will change UART2 Modem control pins to GPIOs.

0	UR2_GP_EN1	R/W	1	Set “1” will change UART2 SIN/SOUT pins to GPIOs. Set UR2_GP_EN1 and UR2_GP_EN2 will also disable UART2.

6.1.13 Multi-Function Select Register 4 — Index 2Bh (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	GPIO47_EN	R/W	0	PSON#/GPIO47 function select. 0: The pin function is PSON#. 1: The pin function is GPIO47.
6	GPIO46_EN	R/W	0	PSOUT#/GPIO46 function select. 0: The pin function is PSOUT#. 1: The pin function is GPIO46.
5	GPIO45_EN	R/W	0	PSIN#/GPIO45 function select. 0: The pin function is PSIN#. 1: The pin function is GPIO45.
4	GPIO44_EN	R/W	0	ATXPG_IN/GPIO44 function select. 0: The pin function is ATXPG_IN. 1: The pin function is GPIO44.
3	GPIO43_EN	R/W	1	GPIO43/IRRX function select. 0: The pin function is IRRX. 1: The pin function is GPIO43.
2	GPIO42_EN	R/W	1	GPIO42/IRTX function select. 0: The pin function is IRTX. 1: The pin function is GPIO42.
1	GPIO41_EN	R/W	1	FANCTRL3/GPIO41 function select. 0: The pin function is FANCTRL3. 1: The pin function is GPIO41.
0	GPIO40_EN	R/W	1	FANIN3/GPIO40 function select. 0: The pin function is FANIN3. 1: The pin function is GPIO40.

6.1.14 Multi-Function Select Register 5 — Index 2Ch (Powered by I_VSB3V)

Bit	Name	R/W	Default	Description
7	TSI_PIN60_EN	R/W	0	Enable pin 60 SDA function. 0: The pin function is GPIO11/PCI_RST5#. 1: The pin function is SDA.
6	TSI_PIN59_EN	R/W	0	Enable pin 59 SCL function. 0: The pin function is GPIO10/PCI_RST4#. 1: The pin function is SCL.
5	TSI_PIN58_EN	R/W	0	Enable pin 58 SDA function. 0: The pin function is PECI. 1: The pin function is SDA.
4	TSI_PIN57_EN	R/W	0	Enable pin 57 SCL function. 0: The pin function is CIR_LED#. 1: The pin function is SCL.
3	GPIO03_EN	R/W	1	CIRRX#/GPIO03 function select. 0: The pin function is CIRRX#. 1: The pin function is GPIO03.
2	GPIO02_EN	R/W	1	CIRTX/GPIO01 function select. 0: The pin function is CIRTX. 1: The pin function is GPIO02.
1	GPIO01_EN	R/W	1	CIRWB#/GPIO01 function select. 0: The pin function is CIRWB#. 1: The pin function is GPIO01.
0	Reserved	R/W	0	Reserved

6.1.15 Wakeup Control Register — Index 2Dh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	SLOT_PWR_SEL	R/W	0	0: SLOTOCC# is pull-up to VSB3V. 1: SLOTOCC# is pull-up to VBAT.
6	VSBOK_HYS_DIS	R/W	0	Set “1” to disable VSBOK hysteresis.

5	VSBOK_LEVEL _SEL	R/W	1	0: The VSB3V Power good level is 3.05V typically. 1: The VSB3V Power good level is 2.8V typically
4	KEY_SEL_ADD	R/W	0	This bit is added to add more wakeup key function.
3	WAKEUP_EN	R/W	1	0: disable keyboard/mouse wake up. 1: enable keyboard/mouse wake up.
2-1	KEY_SEL	R/W	00	This registers select the keyboard wake up key. Accompanying with KEY_SEL_ADD, there are eight wakeup keys:
0	MO_SEL	R/W	0	This register selects the mouse wake up key. 0: Wake up by click. 1: Wake up by click and movement.

KEY_SEL_ADD	KEY_SEL	Wakeup Key
0	00	Ctrl + Esc
0	01	Ctrl + F1
0	10	Ctrl + Space
0	11	Any Key
1	00	Windows Wakeup
1	01	Windows Power
1	10	Ctrl + Alt + Space
1	11	Space

6.2 FDC Registers (CR00)

6.2.1 FDC Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	FDC_EN	R/W	1	0: disable FDC. 1: enable FDC.

6.2.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of FDC base address.

6.2.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	F0h	The LSB of FDC base address.

6.2.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELFDCIRQ	R/W	06h	Select the IRQ channel for FDC.

6.2.5 DMA Channel Select Register — Index 74h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved.
2-0	SELFDCDMA	R/W	010	Select the DMA channel for FDC.

6.2.6 FDD Mode Register — Index F0h

Bit	Name	R/W	Default	Description
7	FDC_SW_PD	R/W	0	Write “1” to software power down FDC.
6-5	Reserved	-	-	Reserved.
4	FDC_SW_WP	R/W	0	Write “1” to this bit will force FDC to write protect. Otherwise, write protect is controlled by hardware pin WP#.
3-2	IF_MODE	R/W	11	00: Model 30 mode. 01: PS/2 mode. 10: Reserved. 11: AT mode (default).
1	FDMAMODE	R/W	1	0: enable burst mode. 1: non-busrt mode (default).
0	EN3MODE	R/W	0	0: normal floppy mode (default). 1: enhanced 3-mode FDD.

6.2.7 FDD Drive Type Register — Index F2h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.
1-0	FDD_TYPE	R/W	11	FDD drive type.

6.2.8 FDD Selection Register — Index F4h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4-3	FDD_DRT	R/W	00	Data rate table select, refer to table A. 00: select regular drives and 2.88 format. 01: 3-mode drive. 10: 2 mega tape. 11: reserved.
2	Reserved	-	-	Reserved.
1-0	FDD_DT	R/W	00	Drive type select, refer to table B.

TABLE A

Data Rate Table Select		Data Rate		Selected Data Rate		DENSEL
FDD_DRT[1]	FDD_DRT[0]	DATARATE1	DATARATE0	MFM	FM	
0	0	0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
		1	1	1Meg	---	1
0	1	0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
		1	1	1Meg	---	1
1	0	0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0
		1	1	1Meg	---	1

Drive Type		DRVDEN0	Remark
FDD_DT1	FDD_DT0		
0	0	DENSEL	4/2/1 MB 3.5” 2/1 MB 5.25” 1/1.6/1 MB 3.5” (
0	1	DATARATE1	
1	0	DENSEL#	
1	1	DATARATE0	

TABLE B

6.3 UART1 Registers (CR01)

6.3.1 UART 1 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR1_EN	R/W	1	0: disable UART 1. 1: enable UART 1.

6.3.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of UART 1 base address.

6.3.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	F8h	The LSB of UART 1 base address.

6.3.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELUR1IRQ	R/W	4h	Select the IRQ channel for UART 1.

6.3.5 RS485 Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	RS485_INV	-	-	Write “1” will invert the RTS# if RS485_EN is set.
4	RS485_EN	R/W	0	0: RS232 driver. 1: RS485 driver. RTS# drive high when transmitting data, otherwise is kept low.
3-0	Reserved	-	-	Reserved.

6.4 UART2 Registers (CR02)

6.4.1 UART 2 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR2_EN	R/W	1	0: disable UART 2. 1: enable UART 2.

6.4.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	02h	The MSB of UART 2 base address.

6.4.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	F8h	The LSB of UART 2 base address.

6.4.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELUR2IRQ	R/W	3h	Select the IRQ channel for UART 2.

6.4.5 RS485 Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	RS485_INV	-	-	Write “1” will invert the RTS# if RS485_EN is set.
4	RS485_EN	R/W	0	0: RS232 driver. 1: RS485 driver. RTS# drive high when transmitting data, otherwise is kept low.
3	RXW4C_IR	R/W	0	0: No reception delay when SIR is changed form TX to RX. 1: Reception delays 4 characters time when SIR is changed form TX to RX.
2	TXW4C_IR	R/W	0	0: No transmission delay when SIR is changed form RX to TX. 1: Transmission delays 4 characters time when SIR is changed form RX to TX.
1-0	Reserved	-	-	Reserved.

6.4.6 SIR Mode Control Register — Index F1h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	Reserved	-	-	Reserved.
5	Reserved	-	-	Reserved.
4-3	IRMODE	R/W	00	00: disable IR function. 01: disable IR function. 10: IrDA function, active pulse is 1.6uS. 11: IrDA function, active pulse is 3/16 bit time.
2	HDUPLX	R/W	1	0: SIR is in full duplex mode for Loopback test. TXW4C_IR and RXW4C_IR are of no use. 1: SIR is in half duplex mode.
1	TXINV_IR	R/W	0	0: IRTX is in normal condition. 1: inverse the IRTX.
0	RXINV_IR	R/W	0	0: IRRX is in normal condition. 1: inverse the IRRX.

6.5 Parallel Port Register (CR03)

6.5.1 Parallel Port Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	PRT_EN	R/W	1	0: disable Parallel Port. 1: enable Parallel Port.

6.5.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of Parallel Port base address.

6.5.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	78h	The LSB of Parallel Port base address.

6.5.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
3-0	SELPRTIRQ	R/W	7h	Select the IRQ channel for Parallel Port.

6.5.5 DMA Channel Select Register — Index 74h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	ECP_DMA_MODE	R/W	0	0: non-burst mode DMA. 1: enable burst mode DMA.
3	Reserved	-	-	Reserved.
2-0	SELPRTDMA	R/W	011	Select the DMA channel for Parallel Port.

6.5.6 PRT Mode Select Register — Index F0h

Bit	Name	R/W	Default	Description
7	SPP_IRQ_MODE	R/W	0	Interrupt mode in non-ECP mode. 0: Level mode. 1: Pulse mode.
6-3	ECP_FIFO_THR	R/W	1000	ECP FIFO threshold.
2-0	PRT_MODE	R/W	010	000: Standard and Bi-direction (SPP) mode. 001: EPP 1.9 and SPP mode. 010: ECP mode (default). 011: ECP and EPP 1.9 mode. 100: Printer mode. 101: EPP 1.7 and SPP mode. 110: Reserved. 111: ECP and EPP1.7 mode.

6.6 Hardware Monitor Registers (CR04)

6.6.1 Hardware Monitor Configuration Registers — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	HM_EN	R/W	1	0: disable Hardware Monitor. 1: enable Hardware Monitor.

6.6.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	02h	The MSB of Hardware Monitor base address.

6.6.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	95h	The LSB of Hardware Monitor base address.

6.6.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELHMIRQ	R/W	0000	Select the IRQ channel for Hardware Monitor.

Before the device registers, the following is a register map order which shows a summary of all registers. Please refer each one register if you want more detail information.

Register CR01 ~ CR03 → Configuration Registers

Register CR0A ~ CR0F → PECI/TSI Control Register

Register CR10 ~ CR37 → Voltage Setting Register

Register CR40 ~ CR4F → PECI 3.0 Command and Register

Register CR60 ~ CR8E → Temperature Setting Register

Register CR90 ~ CRDF → Fan Control Setting Register

→Fan1 Detail Setting CRA0 ~ CRAF

→Fan2 Detail Setting CRB0 ~ CRBF

→Fan3 Detail Setting CRC0 ~ CRCF

6.6.5 Configuration Register — Index 01h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	0	Reserved
2	POWER_DOWN	R/W	0	Hardware monitor function power down.
1	FAN_START	R/W	1	Set one to enable startup of fan monitoring operations; a zero puts the part in standby mode.
0	V_T_START	R/W	1	Set one to enable startup of temperature and voltage monitoring operations; a zero puts the part in standby mode.

6.6.6 Configuration Register — Index 02h

Bit	Name	R/W	Default	Description
7	Reserved	R/W	0	Dummy register.
6	CASE_BEEP_EN	R/W	0	0: Disable case open event output via BEEP. 1: Enable case open event output via BEEP.

5-4	OVT_MODE	R/W	0	00: The OVT# will be low active level mode. 01: The OVT# will be low pulse mode. 10: The OVT# will indicate by 1Hz LED function. 11: The OVT# will indicate by (400/800HZ) BEEP output.
3	Reserved	R/W	0	Dummy register.
2	CASE_SMI_EN	R/W	0	0: Disable case open event output via PME. 1: Enable case open event output via PME.
1-0	ALERT_MODE	R/W	0	00: The ALERT# will be low active level mode. 01: The ALERT# will be high active level mode. 10: The ALERT# will indicate by 1Hz LED function. 11: The ALERT# will indicate by (400/800HZ) BEEP output.

6.6.7 Configuration Register — Index 03h

Bit	Name	R/W	Default	Description
7-1	Reserved	R/W	0	Reserved
0	CASE_STS	R/W	1	Case open event status. Write 1 to clear if case open event cleared. (This bit is powered by VBAT.)

6.6.8 NEW TSI Mode Enable Register Index 07h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	0	Reserved
0	New_TSI_MODE	R/W	0	Set this bit to enable TSI new mode. Please check CR0A for more detail.

6.6.9 Configuration Register — Index 08h

Bit	Name	R/W	Default	Description
7-1	SMBUS_ADDR	R/W	7'h26	When AMD TSI or Intel PCH SMBus is enabled, this byte is used as SMBUS_ADDR. SMBUS_ADDR[7:1] is the slave address sent by the embedded master to fetch the temperature.
0	Reserved	-	-	Reserved

6.6.10 Configuration Register — Index 09h

Bit	Name	R/W	Default	Description
7-1	I2C_ADDR	R/W	0	I2C_ADDR[7:1] is the slave address sent by the embedded master when using a block write command
0	Reserved	R/W	0	Reserved

6.6.11 Configuration Register — Index 0Ah

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td>7</td><td>BETA_EN</td><td>R/W</td><td>0</td><td>0: disable the T1 beta compensation.
1: enable the T1 beta compensation.</td></tr>
<tr><td>6</td><td>INTEL_MODEL</td><td>R/W</td><td>1</td><td>0: AMD model.
1: Intel model.</td></tr>
<tr><td>5</td><td>Reserved</td><td>-</td><td>0</td><td>Reserved.</td></tr>
<tr><td>4</td><td>MXM_MODE</td><td>R/W</td><td>0</td><td>Reserved</td></tr>
<tr><td>3-2</td><td>VTT_SEL</td><td>R/W</td><td>0</td><td>PECI (Vtt) voltage select.
00: Vtt is 1.23V
01: Vtt is 1.13V
10: Vtt is 1.00V
11: Vtt is 1.00V</td></tr>
<tr><td>1</td><td>TSI_EN</td><td>R/W</td><td>0</td><td>0: Disable the TSI function via PECI / CIR_LED / PCI_RST4# / PCI_RST5# pins.
1: Enable the TSI function via PECI / CIR_LED / PCI_RST4# / PCI_RST5# pins.
This bit accompanies with INTEL_MODEL, IBX_ALT_EN, PECI_EN, and it determines the availability of AMD TSI, Intel PCH SMBus, or PECI.
Setting (CR07[0]-- NEW_TSI_MODE = 0)
<table>
<tr><th>INTEL_MODEL (CR0A, bit6)</th><th>TSI_EN (CR0A, bit1)</th><th>PECI_EN (CR0A, bit0)</th><th>IBX_ALT_EN (CR2A, bit6 in global configuration register)</th><th>PECI</th><th>AMD TSI</th><th>Intel PCH SMBus</th></tr>
<tr><td>0</td><td>0</td><td>X</td><td>X</td><td>N</td><td>N</td><td>N</td></tr>
<tr><td>0</td><td>1</td><td>X</td><td>X</td><td>N</td><td>Y</td><td>N</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>X</td><td>Y</td><td>N</td><td>N</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Y</td><td>N</td><td>Y</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>X</td><td>N</td><td>N</td><td>Y</td></tr>
</table>
Setting (CR07[0]-- NEW_TSI_MODE = 1)
<table>
<tr><th>INTEL_MODEL (CR0A, bit6)</th><th>TSI_EN (CR0A, bit1)</th><th>PECI_EN (CR0A, bit0)</th><th>IBX_ALT_EN (CR2A, bit6 in global configuration register)</th><th>PECI</th><th>AMD TSI</th><th>Intel PCH SMBus</th></tr>
<tr><td>0</td><td>0</td><td>X</td><td>X</td><td>N</td><td>N</td><td>N</td></tr>
<tr><td>0</td><td>1</td><td>X</td><td>X</td><td>N</td><td>N</td><td>Y</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>X</td><td>Y</td><td>N</td><td>N</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Y</td><td>Y</td><td>N</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>X</td><td>N</td><td>Y</td><td>N</td></tr>
</table></td></tr>
<tr><td>0</td><td>PECI_EN</td><td>R/W</td><td>0</td><td>0: Disable PECI function via PECI pin
1: Enable PECI function via PECI pin</td></tr>
</table>

6.6.12 Configuration Register — Index 0Bh

Bit	Name	R/W	Default	Description
7-4	CPU_SEL	R/W	0	Select the Intel CPU socket number. 0000: no CPU presented. PECI host will use Ping() command to find CPU address. 0001: CPU is in socket 0, i.e. PECI address is 0x30. 0010: CPU is in socket 0, i.e. PECI address is 0x31. 0100: CPU is in socket 0, i.e. PECI address is 0x32. 1000: CPU is in socket 0, i.e. PECI address is 0x33. Others are reserved.
3-1	Reserved	-	0	Reserved.
0	DOMAIN1_EN	R/W	0	If the CPU is selected as dual core. Set this register 1 to read the temperature of domain1.

6.6.13 Configuration Register — Index 0Ch

Bit	Name	R/W	Default	Description
7-0	TCC_TEMP	R/W	8'h55	TCC Activation Temperature. When PECI is enabled, the absolute value of CPU temperature is calculated by the equation: CPU_TEMP = TCC_TEMP + PECI Reading. The range of this register is -128 ~ 127.

6.6.14 Configuration Register — Index 0Dh

Bit	Name	R/W	Default	Description
7-0	TSI_OFFSET	R/W	8'h00	TSI Temperature offset for CPU When AMD TSI or Intel PCH SMBus is enabled, this byte is used as the offset to be added to the temperature reading of CPU.

6.6.15 Configuration Register — Index 0Fh

Bit	Name	R/W	Default	Description
7-6	Reserved	-	0	Reserved.
5	Reserved	R/W	1	Dummy Register
4-2	Reserved	-	0	Reserved.
1-0	DIG_RATE_SEL	R/W	0	Digital temperatures monitoring rate for PECI, AMD TSI, or Intel PCH SMBus. The rate is calculated by 20Hz/(DIG_RATE_SEL + 1).

6.6.16 Voltage-Protect Shut Down Enable Register — Index 10h

Bit	Name	R/W	Default	Description
7	Reserved	-	0	Reserved.
6	V6_VP_EN	R/W	0	Voltage-Protect shut down enable for VIN6
5	V5_VP_EN	R/W	0	Voltage-Protect enable for VIN5
4-1	Reserved	-	0	Reserved
0	V0_VP_EN	R/W	0	Voltage-Protect shut down enable for 3VCC

6.6.17 Voltage-Protect Status Register (Powered by VBAT) — Index 11h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	0	Reserved.
0	V_EXC_VP	R/WC	0	This bit is voltage-protect status. Once one of the monitored voltages (3VCC, VIN5, VIN6) over its related over-voltage limits or under its related under-voltage limits and if the related voltage-protect shut down enable bit is set, this bit will be set to 1. Write a 1 to this bit will clear it to 0. (This bit is powered by VBAT)

6.6.18 Voltage-Protect Configuration Register (Powered by VBAT) — Index 12h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-2	PU_TIME	R/W	2'h1	PSON# de-active time select in alarm mode of voltage protection. 00: PSON# tri-state 0.5 sec and then inverted of S3# when over voltage or under voltage occurs. 01: PSON# tri-state 1 sec and then inverted of S3# when over voltage or under voltage occurs. 10: PSON# tri-state 2 sec and then inverted of S3# when over voltage or under voltage occurs. 11: PSON# tri-state 4 sec and then inverted of S3# when over voltage or under voltage occurs.
1-0	VP_EN_DELAY	R/W	2'h2	VP_EN_DELAY could set the delay time to start voltage protecting after VDD power is ok when OVP_MODE is 1. (OVP_MODE is strapped by RTS1# pin) 00: bypass 01: 50ms 10: 100ms 11: 200ms

6.6.19 Voltage Protection Power Good Select Register — Index 3Fh

Bit	Name	R/W	Default	Description
7-1	Reserved	--	0	Reserved
0	OVP_RST_SEL	R/W	0	0: OVP/UVP power good signal is VDD3VOK (VCC3V > 2.8V) 1: OVP/UVP power good signal is PWROK. OVP/UVP function wont' start detecting until power good.

6.6.20 Voltage reading and limit— Index 20h- 37h

Address	Attribute	Default Value	Description
20h	R	--	3VCC reading. The unit of reading is 8mV.
21h	R	--	VIN1 (Vcore) reading. The unit of reading is 8mV.
22h	R	--	VIN2 reading. The unit of reading is 8mV.
23h	R	--	VIN3 reading. The unit of reading is 8mV.
24h	R	--	VIN4 reading. The unit of reading is 8mV.
25h	R	--	VIN5 reading. The unit of reading is 8mV.
26h	R	--	VIN6 reading. The unit of reading is 8mV.
27h	R	--	VSB3V reading. The unit of reading is 8mV.
28h	R	--	VBAT reading. The unit of reading is 8mV.
29h	R	FF	Reserved
30h	R/W	7A	3VCC under-voltage limit (V0_UVV_LIMIT). The unit is 9mv (This byte is powered by VBAT)
31h	R/W	D7	3VCC over-voltage limit (V0_OVV_LIMIT). The unit is 9mv. (This byte is powered by VBAT.)
32~35h	R	FF	Reserved
36h	R/W	C9	VIN5 over-voltage limit (V5_OVV_LIMIT). The unit is 9mv. (This byte is powered by VBAT.)
37h	R/W	C8	VIN6 over-voltage limit (V6_OVV_LIMIT). The unit is 9mv. (This byte is powered by VBAT.)
38h	R/W	75	VIN5 under-voltage limit (V5_UVV_LIMIT). The unit is 9mv (This byte is powered by VBAT)
39h	R/W	85	VIN6 under-voltage limit (V6_UVV_LIMIT). The unit is 9mv (This byte is powered by VBAT)
3Fh	W	FF	Write bit 0 to "1" to select OVP start monitor after PWROK ready.

PECI 3.0 Command and Register

6.6.21 PECI Configuration Register — Index 40h

Bit	Name	R/W	Default	Description
7	RDIAMSR_CMD_EN	R/W	0	When PECI temperature monitoring is enabled, set this bit 1 will generate a RdIAMSR() command before a GetTemp() command.
6	C3_UPDATE_EN	R/W	0	If RDIAMSR_CMD_EN is not set to 1, the temperature data is not allowed to be updated when the completion code of RdIAMSR() is 0x82.
5-4	Reserved	R	-	Reserved
3	C3_PTEMP_EN	R/W	0	Set this bit 1 to enable updateing positive value of temperature if the completion code of RdIAMSR() is 0x82.
2	C0_PTEMP_EN	R/W	0	Set this bit 1 to enable updating positive value of temperature if the completion code of RdIAMSR() is not 0x82 and the bit 8 of completion code is not 1 either.
1	C3_ALL0_EN	R/W	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR() is 0x82.
0	C0_ALL0_EN	R/W	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR() is not 0x82 and the bit 8 of completion code is not 1 either.

6.6.22 PECI Master Control Register — Index 41h

Bit	Name	R/W	Default	Description
7	PECI_CMD_START	W	-	Write 1 to this bit to start a PECI command when using as a PECI master. (PECI_PENDING must be set to 1)
6-5	Reserved	R	-	Reserved
4	PECI_PENDING	R/W	0	Set this bit 1 to stop monitoring PECI temperature.
3	Reserved	R	-	Reserved
2-0	PECI_CMD	R/W	3'h0	PECI command to be used by PECI master. 000: PING() 001: GetDIB() 010: GetTemp() 011: RdIAMSR() 100: RdPkgConfig() 101: WrPkgConfig() others: Reserved

6.6.23 PECI Master Status Register — Index 42h

Bit	Name	R/W	Default	Description
7-3	Reserved	R	-	Reserved
2	ABORT_FCS	R/WC	-	This bit is the Abort FCS status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.
1	PECI_FCS_ERR	R/WC	-	This bit is the FCS error status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.
0	PECI_FINISH	R/WC	-	This bit is the Command Finish status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.

6.6.24 PECI Master DATA0 Register — Index 43h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA0	R/W	0	For RdIAMSR(), RdPkgConfig() and WrPkgConfig() command, this byte represents “Host ID[7:1] & Retry[0]”. Please refer to PECI interface specification for more detail.

6.6.25 PECI Master DATA1 Register — Index 44h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA1	R/W	0	For RdIAMSR() , this byte represents “Processor ID”. For RdPkgConfig() and WrPkgConfig() , this byte represents “Index”. Please refer to PECI interface specification for more detail.

6.6.26 PECI Master DATA2 Register — Index 45h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA2	R/W	0	For RdIAMSR(), this byte is the least significant byte of “MSR Address”. For RdPkgConfig() and WrPkgConfig(), this byte is the least significant byte of “Parameter”. Please refer to PECI interface specification for more detail.

6.6.27 PECI Master DATA3 Register — Index 46h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA3	R/W	0	For RdIAMSR(), this byte is the most significant byte of “MSR Address”. For RdPkgConfig() and WrPkgConfig(), this byte is the most significant byte of “Parameter”. Please refer to PECI interface specification for more detail.

6.6.28 PECI Master DATA4 Register — Index 47h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA4	R/W	0	For GetDIB() , this byte represents “Device Info” For GetTemp(), this byte represents the least significant byte of temperature. For RdIAMSR() and RdPkgConfig() , this byte is “Completion Code”. For WrPkgConfig(), this byte represents “DATA[7:0]”

6.6.29 PECI Master DATA5 Register — Index 48h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA5	R/W	0	For GetDIB() , this byte represents “Revision Number” For GetTemp(), this byte represents the most significant byte of temperature. For RdIAMSR() and RdPkgConfig() , this byte represents “DATA[7:0]” For WrPkgConfig(), this byte represents “DATA[15:8]”

6.6.30 PECI Master DATA6 Register — Index 49h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA6	R/W	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[15:8]". For WrPkgConfig(), this byte represents "DATA[23:16]"

6.6.31 PECI Master DATA7 Register — Index 4Ah

Bit	Name	R/W	Default	Description
7-0	PECI_DATA7	R/W	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[23:16]". For WrPkgConfig(), this byte represents "DATA[31:24]"

6.6.32 PECI Master DATA8 Register — Index 4Bh

Bit	Name	R/W	Default	Description
7-0	PECI_DATA8	R/W	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[31:24]". For WrPkgConfig(), this byte represents "AW FCS"

6.6.33 PECI Master DATA9 Register — Index 4Ch

Bit	Name	R/W	Default	Description
7-0	PECI_DATA9	R/W	0	For RdIAMSR(), this byte represents "DATA[39:32]". For WrPkgConfig(), this byte represents "Completion Code"

6.6.34 PECI Master DATA10 Register — Index 4Dh

Bit	Name	R/W	Default	Description
7-0	PECI_DATA10	R/W	0	For RdIAMSR(), this byte represents "DATA[47:40]".

6.6.35 PECI Master DATA11 Register — Index 4Eh

Bit	Name	R/W	Default	Description
7-0	PECI_DATA11	R/W	0	For RdIAMSR(), this byte represents "DATA[55:48]".

6.6.36 PECI Master DATA12 Register — Index 4Fh

Bit	Name	R/W	Default	Description
7-0	PECI_DATA12	R/W	0	For RdIAMSR(), this byte represents "DATA[63:56]".

Temperature Setting

6.6.37 Temperature PME# Enable Register — Index 60h

Bit	Name	R/W	Default	Description
7	EN_ T3_OVT_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP3 exceeds OVT limit setting.
6	EN_ T2_OVT_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds OVT setting.

5	EN_ T1_OVT_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds OVT setting.
4	Reserved	R/W	0	Reserved
3	EN_ T3_EXC_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP3 exceeds high limit setting.
2	EN_ T2_EXC_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds high limit setting.
0	Reserved	R/W	0	Reserved

6.6.38 Temperature Interrupt Status Register — Index 61h

Bit	Name	R/W	Default	Description
7	T3_OVT_STS	R/W	0	This bit gets 1 to indicate TEMP3 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, and write 0 to ignore.
6	T2_OVT _STS	R/W	0	This bit gets 1 to indicate TEMP2 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 to ignore.
5	T1_OVT _STS	R/W	0	This bit gets 1 to indicate TEMP1 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 to ignore.
4	Reserved	R/W	0	Reserved
3	T3_EXC _STS	R/W	0	This bit gets 1 to indicate TEMP3 temperature sensor has exceeded high limit or below the “high limit –hysteresis”. Write 1 to clear this bit, write 0 to ignore.
2	T2_EXC _STS	R/W	0	This bit gets 1 to indicate TEMP2 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 to ignore.
1	T1_EXC _STS	R/W	0	This bit gets 1 to indicate TEMP1 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 to ignore.
0	Reserved	R/W	0	Reserved

6.6.39 Temperature Real Time Status Register — Index 62h

Bit	Name	R/W	Default	Description
7	T3_OVT	R/W	0	Set when the TEMP3 exceeds the OVT limit. Clear when the TEMP3 is below the “OVT limit –hysteresis” temperature.
6	T2_OVT	R/W	0	Set when the TEMP2 exceeds the OVT limit. Clear when the TEMP2 is below the “OVT limit –hysteresis” temperature.
5	T1_OVT	R/W	0	Set when the TEMP1 exceeds the OVT limit. Clear when the TEMP1 is below the “OVT limit –hysteresis” temperature.
4	Reserved	R/W	0	Reserved
3	T3_EXC	R/W	0	Set when the TEMP3 exceeds the high limit. Clear when the TEMP3 is below the “high limit –hysteresis” temperature.
2	T2_EXC	R/W	0	Set when the TEMP2 exceeds the high limit. Clear when the TEMP2 is below the “high limit –hysteresis” temperature.
1	T1_EXC	R/W	0	Set when the TEMP1 exceeds the high limit. Clear when the TEMP1 is below the “high limit –hysteresis” temperature.
0	Reserved	R/W	0	Reserved

6.6.40 Temperature BEEP Enable Register — Index 63h

Bit	Name	R/W	Default	Description
7	EN_T3_ OVT_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP3 exceeds OVT limit setting.
6	EN_ T2_ OVT_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds OVT limit setting.
5	EN_ T1_ OVT_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds OVT limit setting.
4	Reserved	R/W	0	Reserved
3	EN_ T3_EXC_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP3 exceeds high limit setting.
2	EN_ T2_EXC_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds high limit setting.
0	Reserved	R/W	0	Reserved

6.6.41 T1 OVT and High Limit Temperature Select Register — Index 64h

Bit	Name	R/W	Default	Description
7-6	Reserved	R/W	0	Reserved
5-4	OVT_TEMP_SEL	R/W	0	Select the source temperature for T1 OVT Limit. 0: Select T1 to be compared to Temperature 1 OVT Limit. 1: Select CPU temperature from PECI to be compared to Temperature 1 OVT Limit. 2: Select CPU temperature from AMD TSI or Intel PCH SMBus to be compared to Temperature 1 OVT Limit. 3: Select the MAX temperature from Intel PCH SMBus to be compared to Temperature 1 OVT Limit.
3-2	Reserved	R/W	0	Reserved
1-0	HIGH_ TEMP_SEL	R/W	0	Select the source temperature for T1 High Limit. 0: Select T1 to be compared to Temperature 1 High Limit. 1: Select CPU temperature from PECI to be compared to Temperature 1 High Limit. 2: Select CPU temperature from AMD TSI or Intel PCH SMBus to be compared to Temperature 1 High Limit. 3: Select the MAX temperature from Intel PCH SMBus to be compared to Temperature 1 High Limit.

6.6.42 OVT and Alert Output Enable Register 1 — Index 66h

Bit	Name	R/W	Default	Description
7	EN_T3_ALERT	R	0	Enable temperature 3 alert event (asserted when temperature over high limit)
6	EN_T2_ALERT	R	0	Enable temperature 2 alert event (asserted when temperature over high limit)
5	EN_T1_ALERT	R	0	Enable temperature 1 alert event (asserted when temperature over high limit)
4	Reserved	R	0	Reserved.
3	EN_T3_OVT	R/W	0	Enable over temperature (OVT) mechanism of temperature3.
2	EN_T2_OVT	R/W	0	Enable over temperature (OVT) mechanism of temperature2.
1	EN_T1_OVT	R/W	1	Enable over temperature (OVT) mechanism of temperature1.
0	Reserved	R	0h	Reserved.

6.6.43 Reserved —Index 67~69h

Bit	Name	R/W	Default	Description
7-0	Reserved	-	-	Reserved

6.6.44 Temperature Sensor Type Register — Index 6Bh

Bit	Name	R/W	Default	Description
7-4	Reserved	RO	0	Reserved
3	T3_MODE	R/W	1	0: TEMP3 is connected to a thermistor 1: TEMP3 is connected to a BJT.(default)
2	T2_MODE	R/W	1	0: TEMP2 is connected to a thermistor. 1: TEMP2 is connected to a BJT. (default)
1	T1_MODE	R/W	1	0: TEMP1 is connected to a thermistor 1: TEMP1 is connected to a BJT.(default)
0	Reserved	R	0	Reserved

6.6.45 TEMP1 Limit Hystersis Select Register — Index 6Ch

Bit	Name	R/W	Default	Description
7-4	TEMP1_HYS	R/W	4h	Limit hysteresis. (0~15 degree C) Temperature and below the (boundary – hysteresis).
3-0	Reserved	R	0h	Reserved

6.6.46 TEMP2 and TEMP3 Limit Hystersis Select Register — Index 6Dh

Bit	Name	R/W	Default	Description
7-4	TEMP3_HYS	R/W	2h	Limit hysteresis. (0~15 degree C) Temperature and below the (boundary – hysteresis).
3-0	TEMP2_HYS	R/W	4h	Limit hysteresis. (0~15 degree C) Temperature and below the (boundary – hysteresis).

6.6.47 DIODE OPEN Status Register — Index 6Fh

Bit	Name	R/W	Default	Description
7-6	Reserved	R	-	Reserved
5	PECI_OPEN	R	-	When PECI interface is enabled, “1” indicates an error code (0x0080 or 0x0081) is received from PECI slave.
4	TSI_OPEN	R	-	When TSI interface is enabled, “1” indicates the error of not receiving NACK bit or a timeout occurred.
3	T3_DIODE_OPEN	R	-	“1” indicates external diode 3 is open
2	T2_DIODE_OPEN	R	-	“1” indicates external diode 2 is open or short

1	T1_DIODE_OPEN	R	-	“1” indicates external diode 1 is open or short
0	Reserved	R	-	Reserved

6.6.48 Temperature — Index 70h- 8Dh

Address	Attribute	Default Value	Description
70h	Reserved	FFh	Reserved
71h	Reserved	FFh	Reserved
72h	R	--	Temperature 1 reading. The unit of reading is 1ºC.At the moment of reading this register.
73h	R	--	Reserved
74h	R	--	Temperature 2 reading. The unit of reading is 1ºC.At the moment of reading this register.
75h	R	--	Reserved
76h	R	--	Temperature 3 reading. The unit of reading is 1ºC.At the moment of reading this register.
77-79h	R	--	Reserved
7Ah	R	--	The data of CPU temperature from digital interface after IIR filter. (Available if Intel IBX or AMD TSI interface is enabled)
7Bh	R	--	The raw data of PCH temperature from digital interface. (Only available if Intel IBX interface is enabled)
7Ch	R	--	The raw data of MCH read from digital interface. (Only available if Intel IBX interface is enabled)
7Dh	R	--	The raw data of maximum temperature between CPU/PCH/MCH from digital interface. (Only available if Intel IBX interface is enabled)
7Eh	R	--	The data of CPU temperature from digital interface after IIR filter. (Only available if PECI interface is enabled)
7Fh	Reserved	FFh	Reserved
80h	Reserved	FFh	Reserved
81h	Reserved	FFh	Reserved
82h	R/W	64h	Temperature sensor 1 OVT limit. The unit is 1ºC.
83h	R/W	55h	Temperature sensor 1 high limit. The unit is 1ºC.
84h	R/W	64h	Temperature sensor 2 OVT limit. The unit is 1ºC.
85h	R/W	55h	Temperature sensor 2 high limit. The unit is 1ºC.
86h	R/W	55h	Temperature sensor 3 OVT limit. The unit is 1ºC.

87h	R/W	46h	Temperature sensor 3 high limit. The unit is 1ºC.
88-8Bh	R	--	Reserved
8C~8Dh	R	FFH	Reserved

6.6.49 Temperature Filter Select Register —Index 8Eh

Bit	Name	R/W	Default	Description
7-6	IIR-QUEUR3	R/W	1h	The queue time for second filter to quickly update values. 00: 8 times. 01: 12 times. 10: 16 times. (default) 11: 24 times.
5-4	IIR-QUEUR2	R/W	1h	The queue time for second filter to quickly update values. 00: 8 times. 01: 12 times. 10: 16 times. (default) 11: 24 times.
3-2	IIR-QUEUR1	R/W	1h	The queue time for second filter to quickly update values. 00: 8 timers. 01: 12 times. 10: 16 times. (default) 11: 24 times.
1-0	IIR-QUEUR_DIG	R/W	1h	The queue time for second filter to quickly update values. (for CPU temperature from PECI or TSI interface) 00: 8 timers. 01: 12 times. 10: 16 times. (default) 11: 24 times.

Fan Control Setting

6.6.50 FAN PME# Enable Register — Index 90h

Bit	Name	R/W	Default	Description
7-3	Reserved	R	0	Reserved
2	EN_FAN3_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt Set this bit 1 to enable PME# function for Fan3.

1	EN_FAN2_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan2.
0	EN_FAN1_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan1.

6.6.51 FAN Interrupt Status Register — Index 91h

Bit	Name	R/W	Default	Description
7-3	Reserved	R	0	Reserved
2	FAN3_STS	R/W	--	This bit is set when the fan3 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
1	FAN2_STS	R/W	--	This bit is set when the fan2 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
0	FAN1_STS	R/W	--	This bit is set when the fan1 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.

6.6.52 FAN Real Time Status Register — Index 92h

Bit	Name	R/W	Default	Description
7-3	Reserved	--	0	Reserved
2	FAN3_EXC	R	--	This bit set to high mean that fan3 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.
1	FAN2_EXC	R	--	This bit set to high mean that fan2 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.
0	FAN1_EXC	R	--	This bit set to high mean that fan1 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.

6.6.53 FAN BEEP# Enable Register — Index 93h

Bit	Name	R/W	Default	Description
7	FULL_WITH_ T3_EN	R/W	0	Set one will enable FAN to force full speed when T3 over high limit.
6	FULL_WITH_ T2_EN	R/W	0	Set one will enable FAN to force full speed when T2 over high limit.

5	FULL_WITH_ T1_EN	R/W	0	Set one will enable FAN to force full speed when T1 over high limit.
4	Reserved	-	-	Reserved
3	Reserved	-	-	Reserved.
2	EN_FAN3_ BEEP	R/W	0	A one enables the corresponding interrupt status bit for BEEP.
1	EN_FAN2_ BEEP	R/W	0	A one enables the corresponding interrupt status bit for BEEP.
0	EN_FAN1_ BEEP	R/W	0	A one enables the corresponding interrupt status bit for BEEP.

6.6.54 FAN Type Select Register — Index 94h

FAN_PROG_SEL = 0

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5-4	FAN3_TYPE	R/W	2'b 0S	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTRL3 0: FANCTRL3 is pull up by external resistor. 1: FANCTRL3 is pull down by internal 100K resistor.
3-2	FAN2_TYPE	R/W	2'b 0S	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTRL2 0: FANCTRL2 is pull up by external resistor. 1: FANCTRL2 is pull down by internal 100K resistor.
1-0	FAN1_TYPE	R/W	2'b 0S	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTRL1 0: FANCTRL1 is pull up by external resistor. 1: FANCTRL1is pull down by internal 100K resistor.

S: Register default values are decided by trapping.

FAN_PROG_SEL = 1

Bit	Name	R/W	Default	Description
7-0	FAN1_BASE _TEMP	R/W	0	This register is used to set the base temperature for FAN1 temperature adjustment. The FAN1 temperature is calculated according to the equation: Tfan1 = Tnow + (Ta – Tb)*Ct Where Tnow is selected by FAN1_TEMP_SEL_DIG and FAN1_TEMP_SEL. Tb is this register, Ta is selected by TFAN1_ADJ_SEL and Ct is selected by TFAN1_ADJ_UP_RATE/TFAN1_ADJ_DN_RATE. To access this register, FAN_PROG_SEL(CR9F[7]) must set to “1”.

6.6.55 FAN1 Temperature Adjust Rate Register — Index 95h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6-4	TFAN1_ADJ_UP _RATE		3’h0	This selects the weighting of the difference between Ta and Tb if Ta is higher than Tb. 3’h1: 1 (Ct = 1) 3’h2: 1/2 (Ct= 1/2) 3’h3: 1/4 (Ct = 1/4) 3’h4: 1/8 (Ct = 1/8) otherwise: 0 To access this byte, FAN_PROG_SEL must set to “1”.
3	Reserved	-	-	Reserved
2-0	TFAN1_ADJ_DN _RATE	R/W	3’h0	This selects the weighting of the difference between Ta and Tb if Ta is lower than Tb. 3’h1: 1 (Ct = 1) 3’h2: 1/2 (Ct= 1/2) 3’h3: 1/4 (Ct = 1/4) 3’h4: 1/8 (Ct = 1/8) otherwise: 0 To access this byte, FAN_PROG_SEL must set to “1”.

6.6.56 FAN mode Select Register — Index 96h

FAN_PROG_SEL = 0

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved
5-4	FAN3_MODE	R/W	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xC6-0xCE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** defined in 0xC6-0xCE. 10: Manual mode fan control. User can write expected **RPM** count to 0xC2-0xC3, and F71869E will adjust duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control. User can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xC3, and F71869E will output this desired duty or voltage to control fan speed.
3-2	FAN2_MODE	R/W	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xB6-0xBE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** (voltage) defined in 0xB6-0xBE. 10: Manual mode fan control. User can write expected **RPM** count to 0xB2-0xB3, and F71869E will adjust duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xB3, and F71869E will output this desired duty or voltage to control fan speed.
1-0	FAN1_MODE	R/W	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xA6-0xAE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** defined in 0xA6-0xAE. 10: Manual mode fan control, user can write expected **RPM** count to 0xA2-0xA3, and F71869E will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xA3, and F71869E will output this desired duty or voltage to control fan speed.

FAN_PROG_SEL = 1

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2-0	TFAN1_ADJ_SEL	R/W	0h	This selects which temperature to be used as Ta for Fan1 temperature adjustment. 000: PECI (CR7Eh) 001: T1 (CR72h) 010: T2 (CR74h) 011: T3 (CR76h) 100: Digital T1 (CR7Ah) 101: Digital T1 (CR7Bh) 110: Digital T2 (CR7Ch) 111: Digital T3 (CR7Dh) otherwise: Ta will be 0. To access this register FAN_PROG_SEL must set to “1”.

6.6.57 Auto FAN1 and FAN2 Boundary Hystersis Select Register — Index 98h

Bit	Name	R/W	Default	Description
7-4	FAN2_HYS	R/W	4h	Boundary hysteresis. (0~15 degree C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).
3-0	FAN1_HYS	R/W	4h	Boundary hysteresis. (0~15 degree C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

6.6.58 Auto FAN3 Boundary Hystersis Select Register — Index 99h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	FAN3_HYS	R/W	2h	Boundary hysteresis. (0~15 degree C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

6.6.59 Fan3 Control Register — Index 9Ah

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.

6	FREQ_SEL_ADD3	R/W	0	This bit and FAN3_PWM_FREQ_SEL are used to select FAN3 PWM frequency. NEW_FREQ_SEL3 = { FREQ_SEL_ADD3, FAN3_PWM_FREQ_SEL} 00: 23.5 KHz 01: 220 Hz 10: 11.75 KHz 11: 5.875 KHz
5	FREQ_SEL_ADD2	R/W	0	This bit and FAN2_PWM_FREQ_SEL are used to select FAN2 PWM frequency. NEW_FREQ_SEL2 = { FREQ_SEL_ADD2, FAN2_PWM_FREQ_SEL} 00: 23.5 KHz 01: 220 Hz 10: 11.75 KHz 11: 5.875 KHz
4	FREQ_SEL_ADD1	R/W	0	This bit and FAN1_PWM_FREQ_SEL are used to select FAN1 PWM frequency. NEW_FREQ_SEL1 = { FREQ_SEL_ADD1, FAN1_PWM_FREQ_SEL} 00: 23.5 KHz 01: 220 Hz 10: 11.75 KHz 11: 5.875 KHz
3-2	Reserved	R/W	0	Reserved (Keep the value of these two bits “0”)
1	Reserved	R/W	1	Reserved (Keep the value of this bit “1”)
0	FAN3_EXT_EN	R/W	0	Set this bit 1 to enable the function that FAN3 output duty could be adjusted by GPIO53/GPIO54.

6.6.60 Auto Fan Up Speed Update Rate Select Register— Index 9Bh

FAN_PROG_SEL = 0

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5-4	FAN3_UP_RATE	R/W	01	Fan3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

3-2	FAN2_UP_RATE	R/W	01	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_UP_RATE	R/W	01	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

FAN_PROG_SEL = 1

Bit	Name	R/W	Default	Description
7	UP_DN_RATE_EN	R/W	0	0: Fan down rate disable 1: Fan down rate enable
6	DIRECT_LOAD_EN	R/W	0	0: Direct load disable 1: Direct load enable for manual duty mode
5-4	FAN3_DN_RATE	R/W	01	Fan3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
3-2	FAN2_DN_RATE	R/W	01	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_DN_RATE	R/W	01	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

6.6.61 FAN1 and FAN2 START UP DUTY-CYCLE/VOLTAGE — Index 9Ch

Bit	Name	R/W	Default	Description
7-4	FAN2_STOP _DUTY	R/W	5h	When fan start, the FAN_CTRL2 will increase duty-cycle from 0 to this (value x 8) directly. And if fan speed is down, the FAN_CTRL 2 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).
3-0	FAN1_STOP _DUTY	R/W	5h	When fan start, the FAN_CTRL 1 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 1 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

6.6.62 FAN3 START UP DUTY-CYCLE/VOLTAGE — Index 9Dh

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	FAN3_STOP_ DUTY	R/W	5h	When fan start, the FAN_CTRL 3 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 3 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

6.6.63 FAN PROGRAMMABLE DUTY-CYCLE/VOLTAGE LOADED AFTER POWER-ON — Index 9Eh

Bit	Name	R/W	Default	Description
7-0	PROG_DUTY_VAL	R/W	66h	This byte will be immediately loaded as Fan duty value after VDD is powered on if it has been programmed before shut down.

6.6.64 Fan Fault Time Register — Index 9Fh

Bit	Name	R/W	Default	Description
7	FAN_PROG_SEL	R/W	0	Set this bit to “1” will enable accessing registers of other bank.
6	FAN_MNT_SEL	R/W	0	Set this bit to monitor a slower fan.
5	Reserved	-	-	Reserved
4	FULL_DUTY_SEL	R/W	-	0: The Fan Duty is 100% and will be loaded immediately after VDD is powered on if CR9E is not been programmed before shut down. (pull down by external resistor) 1: The Fan Duty is 40% and will be loaded immediately after VDD is powered on if CR9E is not been programmed before shut down. (pull up by internal 47K resistor). This register is power on trap by DTR1#.

3-0	F_FAULT_TIME	R/W	Ah	This register determines the time of fan fault. The condition to cause fan fault event is: When PWM_Duty reaches FFh, if the fan speed count can't reach the fan expect count in time. The unit of this register is 1 second. The default value is 11 seconds. (Set to 0 , means 1 seconds. ; Set to 1, means 2 seconds. Set to 2, means 3 seconds. ….) Another condition to cause fan fault event is fan stop and the PWM duty is greater than the minimum duty programmed by the register index 9C-9Dh.

6.6.65 FAN1 Index A0h~AFh

Address	Attribute	Default Value	Description
A0h	RO	8'h0f	FAN1 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A1h	RO	8'hff	FAN1 count reading (LSB).
A2h	R/W	8'h00	RPM mode(CR96 bit0=0): FAN1 expect speed count value (MSB), in auto fan mode (CR96 bit1➔0) this register is auto updated by hardware. Duty mode(CR96 bit0=1): This byte is reserved byte.
A3h	R/W	8'h01	RPM mode(CR96 bit0=0): FAN1 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit0=1): The Value programming in this byte is duty value. In auto fan mode (CR96 bit1➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
A4h	R/W	8'h03	FAN1 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A5h	R/W	8'hff	FAN1 full speed count reading (LSB).

6.6.66 VT1 BOUNDARY 1 TEMPERATURE – Index A6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TMP1	R/W	3Ch (60°C)	The first boundary temperature for VT1 in temperature mode. When VT1 temperature **exceeds** this boundary, expected FAN1 value will be loaded from segment **1** register (index AAh). When VT1 temperature is **under** this boundary – hysteresis, expected FAN1 value will be loaded from segment **2** register (index ABh). This byte is a 2's complement value ranged from -128'C ~ 127'C.

6.7 VT1 BOUNDARY 2 TEMPERATURE – Index A7

Bit	Name	R/W	Default	Description
7-0	BOUND2TMP1	R/W	32 (50°C)	The 2nd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 2 register (index ABh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 3 register (index ACh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

6.8 VT1 BOUNDARY 3 TEMPERATURE – Index A8h

Bit	Name	R/W	Default	Description
7-0	BOUND3TMP1	R/W	28h (40°C)	The 3rd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 3 register (index ACh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 4 register (index ADh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

6.9 VT1 BOUNDARY 4 TEMPERATURE – Index A9

Bit	Name	R/W	Default	Description
7-0	BOUND4TMP1	R/W	1Eh (30°C)	The 4th BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 4 register (index ADh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 5 register (index AEh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

6.9.1 FAN1 SEGMENT 1 SPEED COUNT – Index AAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED1	R/W	FFh (100%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ((100-X)*32/X 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.9.2 FAN1 SEGMENT 2 SPEED COUNT – Index ABh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED1	R/W	D9h (85%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.9.3 FAN1 SEGMENT 3 SPEED COUNT Register – Index ACh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED1	R/W	B2h (70%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.9.4 FAN1 SEGMENT 4 SPEED COUNT Register – Index ADh

Bit	Name	R/W	Default	Description
7-0	SEC4SPEED1		99h (60%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.9.6 FAN1 SEGMENT 5 SPEED COUNT Register – Index AEh

Bit	Name	R/W	Default	Description
7-0	SEC5PEED1	R/W	80h (50%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.9.7 FAN1 Temperature Mapping Select – Index AFh

Bit	Name	R/W	Default	Description
7	FAN1_TEMP _SEL_DIG	R/W	0	This bit companies with FAN1_TEMP_SEL select the temperature source for controlling FAN1.
6	FAN1_PWM _FREQ_SEL	R/W	0	Set this bit to select FAN2 PWM output frequency. 0: 23.5 kHz 1: 220 Hz
5	FAN1_UP_T_EN	R/W	0	Set 1 to force FAN1 to full speed if any temperature over its high limit.
4	FAN1_ INTERPOLATION_ EN	R/W	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN1_JUMP _HIGH_EN	R/W	1	This register controls the FAN1 duty movement when temperature over highest boundary. 0: The FAN1 duty will increases with the slope selected by FAN1_RATE_SEL register. 1: The FAN1 duty will directly jumps to the value of SEC1SPEED1 register. This bit only activates in duty mode.
2	FAN1_JUMP _LOW_EN	R/W	1	This register controls the FAN1 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN1 duty will decreases with the slope selected by FAN1_RATE_SEL register. 1: The FAN1 duty will directly jumps to the value of SEC2SPEED1 register. This bit only activates in duty mode.

1-0	FAN1_TEMP_SEL	R/W	01	This registers company with FAN1_TEMP_SEL_DIG select the temperature source for controlling FAN1. The following value is comprised by {FAN1_TEMP_SEL_DIG, FAN1_TEMP_SEL} 000: fan1 follows PECI temperature (CR7Eh) 001: fan1 follows temperature 1 (CR72h). 010: fan1 follows temperature 2 (CR74h). 011: fan1 follows temperature 3 (CR76h). 100: fan1 follows IBX/TSI CPU temperature (CR7Ah) 101: fan1 follows IBX PCH temperature (CR7Bh). 110: fan1 follows IBX MCH temperature (CR7Ch). 111: fan1 follows IBX maximum temperature (CR7Dh). Others are reserved.

6.9.8 FAN2 Index B0h~BFh

Address	Attribute	Default Value	Description
B0h	RO	8'h0f	FAN2 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B1h	RO	8'hff	FAN2 count reading (LSB).
B2h	R/W	8'h00	RPM mode(CR96 bit2=0): FAN2 expect speed count value (MSB), in auto fan mode(CR96 bit3➔0) this register is auto updated by hardware. Duty mode(CR96 bit2=1): This byte is reserved byte.
B3h	R/W	8'h01	RPM mode(CR96 bit2=0): FAN2 expect speed count value (LSB) or expect PWM duty , in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit2=1): The Value programming in this byte is duty value. In auto fan mode(CR96 bit3➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
B4h	R/W	8'h03	FAN2 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.

B5h	R/W	8'hff	FAN2 full speed count reading (LSB).

6.9.9 VT2 BOUNDARY 1 TEMPERATURE – Index B6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TMP2	R/W	3Ch (60°C)	The first boundary temperature for VT2 in temperature mode. When VT2 temperature **exceeds** this boundary, FAN2 expect value will load from segment **1** register (index Bah). When VT2 temperature is **under** this boundary – hysteresis, FAN2 expect value will load from segment **2** register (index BAh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

6.10 VT2 BOUNDARY 2 TEMPERATURE – Index B7

Bit	Name	R/W	Default	Description
7-0	BOUND2TMP2	R/W	32 (50°C)	The 2nd BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 2 register (index BBh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 3 register (index BCh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

6.11 VT2 BOUNDARY 3 TEMPERATURE – Index B8h

Bit	Name	R/W	Default	Description
7-0	BOUND3TMP2	R/W	28h (40°C)	The 3rd BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 3 register (index BCh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 4 register (index BDh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

6.12 VT2 BOUNDARY 4 TEMPERATURE – Index B9

Bit	Name	R/W	Default	Description
7-0	BOUND4TMP2	R/W	1Eh (30°C)	The 4th BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 4 register (index BDh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 5 register (index BEh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

6.12.1 FAN2 SEGMENT 1 SPEED COUNT – Index BAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED2	R/W	FFh (100%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.12.2 FAN2 SEGMENT 2 SPEED COUNT – Index BBh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED2	R/W	D9h (85%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.12.3 FAN2 SEGMENT 3 SPEED COUNT Register – Index BCh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED2	R/W	B2h (70%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.12.4 FAN2 SEGMENT 4 SPEED COUNT Register – Index BDh

Bit	Name	R/W	Default	Description
7-0	SEC4SPEED2	R/W	99h (60%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.12.5 FAN2 SEGMENT 5 SPEED COUNT Register – Index BEh

Bit	Name	R/W	Default	Description
7-0	SEC5PEED2	R/W	80h (50%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.12.6 FAN2 Temperature Mapping Select – Index BFh

Bit	Name	R/W	Default	Description
7	FAN2_TEMP_ SEL_DIG	R/W	0	This bit companies with FAN2_TEMP_SEL to select the temperature source for controlling FAN2.
6	FAN2_PWM_ FREQ_SEL	R/W	0	Set this bit to select FAN2 PWM output frequency. 0: 23.5 kHz 1: 220 Hz
5	FAN2_UP_T_EN	R/W	0	Set 1 to force FAN2 to full speed if any temperature over its high limit.
4	FAN2_ INTERPOLATION_EN	R/W	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN2_JUMP_ HIGH_EN	R/W	1	This register controls the FAN2 duty movement when temperature over highest boundary. 0: The FAN2 duty will increases with the slope selected by FAN2_RATE_SEL register. 1: The FAN2 duty will directly jumps to the value of SEC1SPEED2 register. This bit only activates in duty mode.
2	FAN2_JUMP_ LOW_EN	R/W	1	This register controls the FAN2 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN2 duty will decreases with the slope selected by FAN2_RATE_SEL register. 1: The FAN2 duty will directly jumps to the value of SEC2SPEED2 register. This bit only activates in duty mode.

1-0	FAN2_TEMP_SEL	R/W	10	This registers companying with FAN2_TEMP_SEL_DIG select the temperature source for controlling FAN2. The following value is comprised by {FAN2_TEMP_SEL_DIG, FAN2_TEMP_SEL} 000: fan2 follows PECI temperature (CR7Eh) 001: fan2 follows temperature 1 (CR72h). 010: fan2 follows temperature 2 (CR74h). 011: fan2 follows temperature 3 (CR76h). 100: fan2 follows IBEX/TSI CPU temperature (CR7Ah) 101: fan2 follows IBEX PCH temperature (CR7Bh). 110: fan2 follows IBEX MCH temperature (CR7Ch). 111: fan2 follows IBEX maximum temperature (CR7Dh). Otherwise: reserved.

6.12.7 FAN3 Index C0h- CFh

Address	Attribute	Default Value	Description
C0h	RO	8'h0F	FAN3 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C1h	RO	8'hff	FAN3 count reading (LSB).
C2h	R/W	8'h00	RPM mode(CR96 bit4=0): FAN3 expect speed count value (MSB), in auto fan mode(CR96 bit5➔0) this register is auto updated by hardware. Duty mode(CR96 bit4=1): This byte is reserved byte.
C3h	R/W	8'h01	RPM mode(CR96 bit4=0): FAN3 expect speed count value (LSB) or expect PWM duty , in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit4=1): The Value programming in this byte is duty value. In auto fan mode(CR96 bit5➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
C4h	R/W	8'h03	FAN3 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.

C5h	R/W	8'hff	FAN3 full speed count reading (LSB).

6.12.8 VT3 BOUNDARY 1 TEMPERATURE – Index C6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TMP3	R/W	3Ch (60^{o}C)	The first boundary temperature for VT3 in temperature mode. When VT3 temperature **exceeds** this boundary, FAN3 expect value will load from segment **1** register (index CA)h. When VT3 temperature is **under** this boundary – hysteresis, FAN3 expect value will load from segment **2** register (index CAh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

6.13 VT3 BOUNDARY 2 TEMPERATURE – Index C7

Bit	Name	R/W	Default	Description
7-0	BOUND2TMP3	R/W	32 (50^{o}C)	The 2nd BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 2 register (index CBh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 3 register (index CCh). This byte is a 2's complement value ranging from -128 ^{o}C ~ 127 ^{o}C.

6.14 VT3 BOUNDARY 3 TEMPERATURE – Index C8h

Bit	Name	R/W	Default	Description
7-0	BOUND3TMP3	R/W	28h (40^{o}C)	The 3rd BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 3 register (index CCh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 4 register (index CDh). This byte is a 2's complement value ranging from -128 ^{o}C ~ 127 ^{o}C.

6.15 VT3 BOUNDARY 4 TEMPERATURE – Index C9

Bit	Name	R/W	Default	Description
7-0	BOUND4TMP3	R/W	1Eh (30^{o}C)	The 4th BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 4 register (index CDh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 5 register (index CEh). This byte is a 2's complement value ranging from -128 ^{o}C ~ 127 ^{o}C.

6.15.1 FAN3 SEGMENT 1 SPEED COUNT – Index CAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED3	R/W	FFh (100%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.15.2 FAN3 SEGMENT 2 SPEED COUNT – Index CBh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED3	R/W	D9h (85%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.16 FAN3 SEGMENT 3 SPEED COUNT – Index CCh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED3	R/W	B2h (70%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.17 FAN3 SEGMENT 4 SPEED COUNT – Index CDh

Bit	Name	R/W	Default	Description
7-0	SEC4SPEED3	R/W	99h (60%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.18 FAN3 SEGMENT 5 SPEED COUNT – Index CEh

Bit	Name	R/W	Default	Description
7-0	SEC5SPEED3	R/W	80h (50%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.18.1 FAN3 Temperature Mapping Select – Index CFh

Bit	Name	R/W	Default	Description
7	FAN3_TEMP_ SEL_DIG	R/W	0	This bit companies with FAN3_TEMP_SEL select the temperature source for controlling FAN3.
6	FAN3_PWM_ FREQ_SEL	R/W	0	Set this bit to select FAN3 PWM output frequency. 0: 23.5 kHz 1: 220 Hz
5	FAN3_UP_T_EN	R/W	0	Set 1 to force FAN3 to full speed if any temperature over its high limit.
4	FAN3_ INTERPOLATION_EN	R/W	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN3_JUMP_ HIGH_EN	R/W	1	This register controls the FAN3 duty movement when temperature over highest boundary. 0: The FAN3 duty will increases with the slope selected by FAN3_RATE_SEL register. 1: The FAN3 duty will directly jumps to the value of SEC1SPEED3 register. This bit only activates in duty mode.
2	FAN3_JUMP_ LOW_EN	R/W	1	This register controls the FAN3 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN3 duty will decreases with the slope selected by FAN3_RATE_SEL register. 1: The FAN3 duty will directly jumps to the value of SEC2SPEED3 register. This bit only activates in duty mode.
1-0	FAN3_TEMP_SEL	R/W	11	This registers companying with FAN3_TEMP_SEL_DIG select the temperature source for controlling FAN3. The following value is comprised by {FAN3_TEMP_SEL_DIG, FAN3_TEMP_SEL} 000: fan3 follows PECI temperature (CR7Eh) 001: fan3 follows temperature 1 (CR72h). 010: fan3 follows temperature 2 (CR74h). 011: fan3 follows temperature 3 (CR76h). 100: fan3 follows IBEX/TSI CPU temperature (CR7Ah) 101: fan3 follows IBEX PCH temperature (CR7Bh). 110: fan3 follows IBEX MCH temperature (CR7Ch). 111: fan3 follows IBEX maximum temperature (CR7Dh). Otherwise: reserved.

6.18.2 TSI Temperature 0 – Index E0h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP0	R/W	-	This is the AMD TSI reading if AMD TSI enable. And will be highest temperature among CPU, MCH and PCH if Intel temperature interface enable. The range is 0~255'C. To access this byte, MCH_BANK_SEL must set to "0".
	SMB_DATA0	R/W	8'h00	This byte is used as multi-purpose: 1. The received data of receive protocol. 2. The first received byte of read word protocol. 3. The 10th received byte of read block protocol. 4. The sent data for send byte protocol and write byte protocol. 5. The first send byte for write word protocol. 6. The first send byte for write block protocol. To access this byte, MCH_BANK_SEL should be set to "1".

6.18.3 TSI Temperature 1 – Index E1h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP1	R	-	This is the high byte of Intel temperature interface PCH reading. The range is 0~255'C. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA1	R/W	8'h00	This byte is used as multi-purpose: 1. The second received byte of read word protocol. 2. The 11th received byte of read block protocol. 3. The second send byte for write word protocol. 4. The second send byte for write block protocol. To access this byte, MCH_BANK_SEL should be set to "1".

6.18.4 TSI Temperature 2 Low Byte – Index E2h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP2_LO	R	-	This is the low byte of Intel temperature interface CPU reading. The reading is the fraction part of CPU temperature. Bit 0 indicates the error status. 0: No error. 1: Error code. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA2	R/W	8'h00	This is the 12th byte of the block read protocol. This byte is also used as the 3rd byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

6.18.5 TSI Temperature 2 High Byte – Index E3h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP2_HI	R	-	This is the high byte of Intel temperature interface CPU reading. The reading is the decimal part of CPU temperature. To access this byte, MCH_BANK_SEL should be set to “0”.
	SMB_DATA3	R/W	8’h00	This is the 13th byte of the block read protocol. This byte is also used as the 4th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to “1”.

6.18.6 TSI Temperature 3 – Index E4h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP3	R	-	This is the high byte of Intel temperature interface MCH reading. The range is 0~255’C. To access this byte, MCH_BANK_SEL should be set to “0”.
	SMB_DATA4	R/W	8’h00	This is the 14th byte of the block read protocol. This byte is also used as the 5th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to “1”.

6.18.7 TSI Temperature 4 – Index E5h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP4	R	-	This is the high byte of Intel temperature interface DIMM0 reading. The range is 0~255’C. To access this byte, MCH_BANK_SEL should be set to “0”.
	SMB_DATA5	R/W	8’h00	This is the 15th byte of the block read protocol. This byte is also used as the 6th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to “1”.

6.18.8 TSI Temperature 5 – Index E6h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP5	R	-	This is the high byte of Intel temperature interface DIMM1 reading. The range is 0~255’C. To access this byte, MCH_BANK_SEL should be set to “0”.
	SMB_DATA6	R/W	8’h00	This is the 16th byte of the block read protocol. This byte is also used as the 7th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to “1”.

6.18.9 TSI Temperature 6 – Index E7h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP6	R	-	This is the high byte of Intel temperature interface DIMM2 reading. The range is 0~255'C. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA7	R/W	8'h00	This is the 17th byte of the block read protocol. This byte is also used as the 8th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

6.18.10 TSI Temperature 7 – Index E8h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP7	R	-	This is the high byte of Intel temperature interface DIMM3 reading. The range is 0~255'C. The above 9 bytes could also be used as the read data of block read protocol if the TSI is disable or pending.
	SMB_DATA8	R/W	8'h00	This is the 18th byte of the block read protocol. This byte is also used as the 9th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

6.18.11 SMB Data Buffer 9 – Index E9h

Bit	Name	R/W	Default	Description
7-0	SMB_DATA9	R/W	FFh	This is the 18th byte of the block read protocol. This byte is also used as the 9th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

6.18.12 Block Write Count Register – Index ECh

Bit	Name	R/W	Default	Description
7	MCH_BANK_SEL	R/W	0	This bit is used to select the register in index E0h to E9h. Set "0" to read the temperature bank and "1" to access the data bank.
6	Reserved	-	0	Reserved
5-0	BLOCK_WR_CNT	R/W	0	Use the register to specify the byte count of block write protocol. Support up to 10 bytes.

6.18.13 SMB Command Byte/TSI Command Byte – Index EDh

Bit	Name	R/W	Default	Description
7-0	SMB_CMD/TSI_CMD	R/W	0/1	There are actual two bytes for this index. TSI_CMD_PROG select which byte to be programmed: 0: SMB_CMD, which is the command code for write byte/word, read byte/word, block write/read and process call protocol. 1: TSI_CMD, which is the command code for Intel temperature interface block read protocol and the data byte for AMD TSI send byte protocol.

6.18.14 SMB Status – Index EEh

Bit	Name	R/W	Default	Description
7	TSI_PENDING	R/W	0	Set 1 to pending auto TSI accessing. (In AMD model, auto accessing will issue a send-byte followed a receive-byte; In Intel model, auto accessing will issue a block read). To use the SCL/ SDA as a SMBus master, set this bit to “1” first.
6	TSI_CMD_PROG	R/W	0	Set 1 to program TSI_CMD.
5	PROC_KILL	R/W	0	Kill the current SMBus transfer and return the state machine to idle. It will set an fail status if the current transfer is not completed.
4	FAIL_STS	R	0	This is set when PROC_KI LL kill an un-completed transfer. It will be auto cleared by next SMBus transfer.
3	SMB_ABT_ERR	R	0	This is the arbitration lost status if a SMBus command is issued. Auto cleared by next SMBus command.
2	SMB_TO_ERR	R	0	This is the timeout status if a SMBus command is issued. Auto cleared by next SMBus command.
1	SMB_NAC_ERR	R	0	This is the NACK error status if a SMBus command is issued. Auto cleared by next SMBus command.
0	SMB_READY	R	1	0: a SMBus transfer is in process. 1: Ready for next SMBus command.

6.18.15 SMB Protocol Select – Index EFh

Bit	Name	R/W	Default	Description
7	SMB_START	W	0	Write “1” to trigger a SMBus transfer with the protocol specified by SMB_PROTOCOL.
6-4	Reserved	-	-	Reserved.

3-0	SMB_PROTOCOL	R/W	0	Select what protocol if a SMBus transfer is triggered. 0001b: send byte. 0010b: write byte. 0011b: write word. 0100b: Reserved. 0101b: block write. 0111b: quick command (write). 1001b: receive byte. 1010b: read byte. 1011b: Reserved 1101b: block read. 1111b: Reserved Otherwise: reserved.

6.19 KBC Registers (CR05)

6.19.1 KBC Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	KBC_EN	R/W	1	0: disable KBC. 1: enable KBC.

6.19.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of KBC command port address. The address of data port is command port address + 4;

6.19.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	60h	The LSB of KBC command port address. The address of data port is command port address + 4.

6.19.4 KBC IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELKIRQ	R/W	1h	Select the IRQ channel for keyboard interrupt.

6.19.5 Mouse IRQ Channel Select Register — Index 72h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELMIRQ	R/W	Ch	Select the IRQ channel for PS/2 mouse interrupt.

6.19.6 Auto Swap Register — Index FEh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	AUTO_DET_EN	R/W	0	0: disable auto detect keyboard/mouse swap. 1: enable auto detect keyboard/mouse swap.
6-5	Reserved	-	-	Reserved.
4	KB_MO_SWAP	R/W	0	0: Keyboard/mouse not swap. 1: Keyboard/mouse swap. This bit is set/clear by hardware if AUTO_DET_EN is set to “1”. Users could also program this bit manually.
3-0	Reserved	-	1h	Reserved

6.19.7 User Wakeup Code Register — Index FEh (Powered by VBAT)

Bit	Name	R/W	Default	Description
9-0	USER_WAKEUP_CODE	R/W	29h	User defined wakeup code.

6.20 GPIO Registers (CR06)

6.20.1 GPIO Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	GPIO_EN	R/W	0	0: disable GPIO I/O Port. 1: enable GPIO I/O Port.

6.20.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of GPIO index/data port address. The index port is BASE_ADDR[15:2] + 5 and the data port is BASE_ADDR[15:2] + 6.

6.20.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	00h	The LSB of GPIO index/data port address. The index port is BASE_ADDR[15:2] + 5 and the data port is BASE_ADDR[15:2] + 6.

6.20.4 GPIRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELGPIRQ	R/W	0h	Select the IRQ channel for GPIO interrupt.

6.20.5 GPIO0 Output Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	GPIO05_OE	R/W	0	0: GPIO05 is in input mode. 1: GPIO05 is in output mode.
4	GPIO04_OE	R/W	0	0: GPIO04 is in input mode. 1: GPIO04 is in output mode.
3	GPIO03_OE	R/W	0	0: GPIO03 is in input mode. 1: GPIO03 is in output mode.
2	GPIO02_OE	R/W	0	0: GPIO02 is in input mode. 1: GPIO02 is in output mode.
1	GPIO01_OE	R/W	0	0: GPIO01 is in input mode. 1: GPIO01 is in output mode.
0	GPIO00_OE	R/W	0	0: GPIO00 is in input mode. 1: GPIO00 is in output mode.

6.20.6 GPIO0 Output Data Register — Index F1h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	GPIO05_VAL	R/W	1	0: GPIO05 outputs 0 when in output mode. 1: GPIO05 outputs 1 when in output mode.
4	GPIO04_VAL	R/W	1	0: GPIO04 outputs 0 when in output mode. 1: GPIO04 outputs 1 when in output mode.
3	GPIO03_VAL	R/W	1	0: GPIO03 outputs 0 when in output mode. 1: GPIO03 outputs 1 when in output mode.
2	GPIO02_VAL	R/W	1	0: GPIO02 outputs 0 when in output mode. 1: GPIO02 outputs 1 when in output mode.
1	GPIO01_VAL	R/W	1	0: GPIO01 outputs 0 when in output mode. 1: GPIO01 outputs 1 when in output mode.
0	GPIO00_VAL	R/W	1	0: GPIO00 outputs 0 when in output mode. 1: GPIO00 outputs 1 when in output mode.

6.20.7 GPIO Pin Status Register — Index F2h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	GPIO05_IN	R	-	The pin status of 3VSBSW/GPIO05
4	GPIO04_IN	R	-	The pin status of SLOTOCC#/GPIO04

3	GPIO03_IN	R	-	The pin status of TIMING1/GPIO03
2	GPIO02_IN	R	-	The pin status of TIMING2/GPIO02
1	GPIO01_IN	R	-	The pin status of TIMING4/GPIO01
0	GPIO00_IN	R	-	The pin status of TIMING3/GPIO00

6.20.8 GPIO Drive Enable Register — Index F3h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
5	GPIO05_DRV_EN	R/W	0	0: GPIO05 is open drain in output mode. 1: GPIO05 is push pull in output mode.
4	GPIO04_DRV_EN	R/W	0	0: GPIO04 is open drain in output mode. 1: GPIO04 is push pull in output mode.
3	GPIO03_DRV_EN	R/W	0	0: GPIO03 is open drain in output mode. 1: GPIO03 is push pull in output mode.
2	GPIO02_DRV_EN	R/W	0	0: GPIO02 is open drain in output mode. 1: GPIO02 is push pull in output mode.
1	GPIO01_DRV_EN	R/W	0	0: GPIO01 is open drain in output mode. 1: GPIO01 is push pull in output mode.
0	GPIO00_DRV_EN	R/W	0	0: GPIO00 is open drain in output mode. 1: GPIO00 is push pull in output mode.

6.20.9 GPIO1 Output Enable Register — Index E0h

Bit	Name	R/W	Default	Description
7	GPIO17_OE	R/W	0	0: GPIO17 is in input mode. 1: GPIO17 is in output mode.
6	GPIO16_OE	R/W	0	0: GPIO16 is in input mode. 1: GPIO16 is in output mode.
5	GPIO15_OE	R/W	0	0: GPIO15 is in input mode. 1: GPIO15 is in output mode.
4	GPIO14_OE	R/W	0	0: GPIO14 is in input mode. 1: GPIO14 is in output mode.
3	GPIO13_OE	R/W	0	0: GPIO13 is in input mode. 1: GPIO13 is in output mode.
2	GPIO12_OE	R/W	0	0: GPIO12 is in input mode. 1: GPIO12 is in output mode.
1	GPIO11_OE	R/W	0	0: GPIO11 is in input mode. 1: GPIO11 is in output mode.
0	GPIO10_OE	R/W	0	0: GPIO10 is in input mode. 1: GPIO10 is in output mode.

6.20.10 GPIO1 Output Data Register — Index E1h

Bit	Name	R/W	Default	Description
7	GPIO17_VAL	R/W	1	0: GPIO17 outputs 0 when in output mode. 1: GPIO17 outputs1 when in output mode.

6	GPIO16_VAL	R/W	1	0: GPIO16 outputs 0 when in output mode. 1: GPIO16 outputs1 when in output mode.
5	GPIO15_VAL	R/W	1	0: GPIO15 outputs 0 when in output mode. 1: GPIO15 outputs 1 when in output mode.
4	GPIO14_VAL	R/W	1	0: GPIO14 outputs 0 when in output mode. 1: GPIO14 outputs 1 when in output mode.
3	GPIO13_VAL	R/W	1	0: GPIO13 outputs 0 when in output mode. 1: GPIO13 outputs 1 when in output mode.
2	GPIO12_VAL	R/W	1	0: GPIO12 outputs 0 when in output mode. 1: GPIO12 outputs 1 when in output mode.
1	GPIO11_VAL	R/W	1	0: GPIO11 outputs 0 when in output mode. 1: GPIO11 outputs 1 when in output mode.
0	GPIO10_VAL	R/W	1	0: GPIO10 outputs 0 when in output mode. 1: GPIO10 outputs 1 when in output mode.

6.20.11 GPIO1 Pin Status Register — Index E2h

Bit	Name	R/W	Default	Description
7	GPIO17_IN	R	-	The pin status of CPU_PWGD/GPIO17.
6	GPIO16_IN	R	-	The pin status of LED_VCC/GPIO16.
5	GPIO15_IN	R	-	The pin status of LED_VSB/ALERT#/GPIO15.
4	GPIO14_IN	R	-	The pin status of WDTRST#/GPIO14.
3	GPIO13_IN	R	-	The pin status of BEEP/GPIO13.
2	GPIO12_IN	R	-	The pin status of RSTCON#/GPIO12.
1	GPIO11_IN	R	-	The pin status of PCI_RST5#/GPIO11.
0	GPIO10_IN	R	-	The pin status of PCI_RST4#/GPIO10.

6.20.12 GPIO1 Drive Enable Register — Index E3h

Bit	Name	R/W	Default	Description
7	GPIO17_DRV_EN	R/W	0	0: GPIO17 is open drain in output mode. 1: GPIO17 is push pull in output mode.
6	GPIO16_DRV_EN	R/W	0	0: GPIO16 is open drain in output mode. 1: GPIO16 is push pull in output mode.
5	GPIO15_DRV_EN	R/W	0	0: GPIO15 is open drain in output mode. 1: GPIO15 is push pull in output mode.
4	GPIO14_DRV_EN	R/W	0	0: GPIO14 is open drain in output mode. 1: GPIO14 is push pull in output mode.
3	GPIO13_DRV_EN	R/W	0	0: GPIO13 is open drain in output mode. 1: GPIO13 is push pull in output mode.
2	GPIO12_DRV_EN	R/W	0	0: GPIO12 is open drain in output mode. 1: GPIO12 is push pull in output mode.
1	GPIO11_DRV_EN	R/W	0	0: GPIO11 is open drain in output mode. 1: GPIO11 is push pull in output mode.
0	GPIO10_DRV_EN	R/W	0	0: GPIO10 is open drain in output mode. 1: GPIO10 is push pull in output mode.

6.20.13 GPIO1 PME Enable Register — Index E4h

Bit	Name	R/W	Default	Description
7	GPIO17_PME_EN	R/W	0	When GPIO17_EVENT_STS is 1 and GPIO17_PME_EN is set to 1, a GPIO PME event will be generated.
6	GPIO16_PME_EN	R/W	0	When GPIO16_EVENT_STS is 1 and GPIO16_PME_EN is set to 1, a GPIO PME event will be generated.
5	GPIO15_PME_EN	R/W	0	When GPIO15_EVENT_STS is 1 and GPIO15_PME_EN is set to 1, a GPIO PME event will be generated.
4	GPIO14_PME_EN	R/W	0	When GPIO14_EVENT_STS is 1 and GPIO14_PME_EN is set to 1, a GPIO PME event will be generated.
3	GPIO13_PME_EN	R/W	0	When GPIO13_EVENT_STS is 1 and GPIO13_PME_EN is set to 1, a GPIO PME event will be generated.
2	GPIO12_PME_EN	R/W	0	When GPIO12_EVENT_STS is 1 and GPIO12_PME_EN is set to 1, a GPIO PME event will be generated.
1	GPIO11_PME_EN	R/W	0	When GPIO11_EVENT_STS is 1 and GPIO11_PME_EN is set to 1, a GPIO PME event will be generated.
0	GPIO10_PME_EN	R/W	0	When GPIO10_EVENT_STS is 1 and GPIO10_PME_EN is set to 1, a GPIO PME event will be generated.

6.20.14 GPIO1 Input Detection Select Register — Index E5h

Bit	Name	R/W	Default	Description
7	GPIO17_DET_SEL	R/W	0	When GPIO17 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
6	GPIO16_DET_SEL	R/W	0	When GPIO16 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
5	GPIO15_DET_SEL	R/W	0	When GPIO15 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
4	GPIO14_DET_SEL	R/W	0	When GPIO14 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
3	GPIO13_DET_SEL	R/W	0	When GPIO13 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
2	GPIO12_DET_SEL	R/W	0	When GPIO12 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge

1	GPIO11_DET_SEL	R/W	0	When GPIO11 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
0	GPIO10_DET_SEL	R/W	0	When GPIO10 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge

6.20.15 GPIO1 Event Status Register — Index E6h

Bit	Name	R/W	Default	Description
7	GPIO17_ EVENT_STS	R/W	0	When GPIO17 is in input mode and a GPIO17 input is detected according to CRE5[7], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
6	GPIO16_ EVENT_STS	R/W	0	When GPIO16 is in input mode and a GPIO16 input is detected according to CRE5[6], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	GPIO15_ EVENT_STS	R/W	0	When GPIO15 is in input mode and a GPIO15 input is detected according to CRE5[5], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
4	GPIO14_ EVENT_STS	R/W	0	When GPIO14 is in input mode and a GPIO14 input is detected according to CRE5[4], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
3	GPIO13_ EVENT_STS	R/W	0	When GPIO13 is in input mode and a GPIO13 input is detected according to CRE5[3], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
2	GPIO12_ EVENT_STS	R/W	0	When GPIO12 is in input mode and a GPIO12 input is detected according to CRE5[2], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
1	GPIO11_ EVENT_STS	R/W	0	When GPIO11 is in input mode and a GPIO11 input is detected according to CRE5[1], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
0	GPIO10_ EVENT_STS	R/W	0	When GPIO10 is in input mode and a GPIO10 input is detected according to CRE5[0], this bit will be set to 1. Write a 1 to this bit will clear it to 0.

6.20.16 GPIO2 Output Enable Register — Index D0h

Bit	Name	R/W	Default	Description
7	GPIO27_OE	R/W	0	0: GPIO27 is in input mode. 1: GPIO27 is in output mode.
6	GPIO26_OE	R/W	0	0: GPIO26 is in input mode. 1: GPIO25 is in output mode.
5	GPIO25_OE	R/W	0	0: GPIO25 is in input mode. 1: GPIO25 is in output mode.
4	GPIO24_OE	R/W	0	0: GPIO24 is in input mode. 1: GPIO24 is in output mode.
3	GPIO23_OE	R/W	0	0: GPIO23 is in input mode. 1: GPIO23 is in output mode.

2	GPIO22_OE	R/W	0	0: GPIO22 is in input mode. 1: GPIO22 is in output mode.
1	GPIO21_OE	R/W	0	0: GPIO21 is in input mode. 1: GPIO21 is in output mode.
0	GPIO20_OE	R/W	0	0: GPIO20 is in input mode. 1: GPIO20 is in output mode.

6.20.17 GPIO2 Output Data Register — Index D1h

Bit	Name	R/W	Default	Description
7	GPIO27_VAL	R/W	1	0: GPIO27 outputs 0 when in output mode. 1: GPIO27 outputs 1 when in output mode.
6	GPIO26_VAL	R/W	1	0: GPIO26 outputs 0 when in output mode. 1: GPIO26 outputs 1 when in output mode.
5	GPIO25_VAL	R/W	1	0: GPIO25 outputs 0 when in output mode. 1: GPIO25 outputs 1 when in output mode.
4	GPIO24_VAL	R/W	1	0: GPIO24 outputs 0 when in output mode. 1: GPIO24 outputs 1 when in output mode.
3	GPIO23_VAL	R/W	1	0: GPIO23 outputs 0 when in output mode. 1: GPIO23 outputs 1 when in output mode.
2	GPIO22_VAL	R/W	1	0: GPIO22 outputs 0 when in output mode. 1: GPIO22 outputs 1 when in output mode.
1	GPIO21_VAL	R/W	1	0: GPIO21 outputs 0 when in output mode. 1: GPIO21 outputs 1 when in output mode.
0	GPIO20_VAL	R/W	1	0: GPIO20 outputs 0 when in output mode. 1: GPIO20 outputs 1 when in output mode.

6.20.18 GPIO2 Pin Status Register — Index D2h

Bit	Name	R/W	Default	Description
7	GPIO27_IN	R	-	The pin status of SIN2/GPIO27.
6	GPIO26_IN	R	-	The pin status of SOUT2/GPIO26.
5	GPIO25_IN	R	-	The pin status of DSR2#/GPIO25.
4	GPIO24_IN	R	-	The pin status of RTS2#/GPIO24.
3	GPIO23_IN	R	-	The pin status of DTR2#/GPIO23.
2	GPIO22_IN	R	-	The pin status of CTS2#/GPIO22.
1	GPIO21_IN	R	-	The pin status of RI2#/GPIO21.
0	GPIO20_IN	R	-	The pin status of DCD2#/GPIO20.

6.20.19 GPIO2 Drive Enable Register — Index D3h

Bit	Name	R/W	Default	Description
7	GPIO27_DRV_EN	R/W	0	0: GPIO27 is open drain in output mode. 1: GPIO27 is push pull in output mode.
6	GPIO26_DRV_EN	R/W	0	0: GPIO26 is open drain in output mode. 1: GPIO26 is push pull in output mode.
5	GPIO25_DRV_EN	R/W	0	0: GPIO25 is open drain in output mode. 1: GPIO25 is push pull in output mode.

4	GPIO24_DRV_EN	R/W	0	0: GPIO24 is open drain in output mode. 1: GPIO24 is push pull in output mode.
3	GPIO23_DRV_EN	R/W	0	0: GPIO23 is open drain in output mode. 1: GPIO23 is push pull in output mode.
2	GPIO22_DRV_EN	R/W	0	0: GPIO22 is open drain in output mode. 1: GPIO22 is push pull in output mode.
1	GPIO21_DRV_EN	R/W	0	0: GPIO21 is open drain in output mode. 1: GPIO21 is push pull in output mode.
0	GPIO20_DRV_EN	R/W	0	0: GPIO20 is open drain in output mode. 1: GPIO20 is push pull in output mode.

6.20.20 GPIO3 Output Enable Register — Index C0h

Bit	Name	R/W	Default	Description
7	GPIO37_OE	R/W	0	0: GPIO37 is in input mode. 1: GPIO37 is in output mode. (Open-drain).
6	GPIO36_OE	R/W	0	0: GPIO36 is in input mode. 1: GPIO35 is in output mode. (Open-drain).
5	GPIO35_OE	R/W	0	0: GPIO35 is in input mode. 1: GPIO35 is in output mode. (Open-drain).
4	GPIO34_OE	R/W	0	0: GPIO34 is in input mode. 1: GPIO34 is in output mode. (Open-drain).
3	GPIO33_OE	R/W	0	0: GPIO33 is in input mode. 1: GPIO33 is in output mode. (Open-drain).
2	GPIO32_OE	R/W	0	0: GPIO32 is in input mode. 1: GPIO32 is in output mode. (Open-drain).
1	GPIO31_OE	R/W	0	0: GPIO31 is in input mode. 1: GPIO31 is in output mode. (Open-drain).
0	GPIO30_OE	R/W	0	0: GPIO30 is in input mode. 1: GPIO30 is in output mode. (Open-drain).

6.20.21 GPIO3 Output Data Register — Index C1h

Bit	Name	R/W	Default	Description
7	GPIO37_VAL	R/W	1	0: GPIO37 outputs 0 when in output mode. 1: GPIO37 outputs 1 when in output mode.
6	GPIO36_VAL	R/W	1	0: GPIO36 outputs 0 when in output mode. 1: GPIO36 outputs 1 when in output mode.
5	GPIO35_VAL	R/W	1	0: GPIO35 outputs 0 when in output mode. 1: GPIO35 outputs 1 when in output mode.
4	GPIO34_VAL	R/W	1	0: GPIO34 outputs 0 when in output mode. 1: GPIO34 outputs 1 when in output mode.
3	GPIO33_VAL	R/W	1	0: GPIO33 outputs 0 when in output mode. 1: GPIO33 outputs 1 when in output mode.
2	GPIO32_VAL	R/W	1	0: GPIO32 outputs 0 when in output mode. 1: GPIO32 outputs 1 when in output mode.
1	GPIO31_VAL	R/W	1	0: GPIO31 outputs 0 when in output mode. 1: GPIO31 outputs 1 when in output mode.

0	GPIO30_VAL	R/W	1	0: GPIO30 outputs 0 when in output mode. 1: GPIO30 outputs 1 when in output mode.

6.20.22 GPIO3 Pin Status Register — Index C2h

Bit	Name	R/W	Default	Description
7	GPIO37_IN	R	-	The pin status of WGATE#/GPIO37.
6	GPIO36_IN	R	-	The pin status of HDSEL#/GPIO36.
5	GPIO35_IN	R	-	The pin status of STEP#/GPIO35.
4	GPIO34_IN	R	-	The pin status of DIR#/GPIO34.
3	GPIO33_IN	R	-	The pin status of WDATA#/GPIO3.
2	GPIO32_IN	R	-	The pin status of DRVA#/GPIO32.
1	GPIO31_IN	R	-	The pin status of MOA#/GPIO31.
0	GPIO30_IN	R	-	The pin status of DENSEL#/GPIO30.

6.20.23 GPIO4 Output Enable Register — Index B0h

Bit	Name	R/W	Default	Description
7	GPIO47_OE	R/W	0	0: GPIO47 is in input mode. 1: GPIO47 is in output mode.
6	GPIO46_OE	R/W	0	0: GPIO46 is in input mode. 1: GPIO46 is in output mode.
5	GPIO45_OE	R/W	0	0: GPIO45 is in input mode. 1: GPIO45 is in output mode.
4	GPIO44_OE	R/W	0	0: GPIO44 is in input mode. 1: GPIO44 is in output mode.
3	GPIO43_OE	R/W	0	0: GPIO43 is in input mode. 1: GPIO43 is in output mode.
2	GPIO42_OE	R/W	0	0: GPIO42 is in input mode. 1: GPIO42 is in output mode.
1	GPIO41_OE	R/W	0	0: GPIO41 is in input mode. 1: GPIO41 is in output mode.
0	GPIO40_OE	R/W	0	0: GPIO40 is in input mode. 1: GPIO40 is in output mode.

6.20.24 GPIO4 Output Data Register — Index B1h

Bit	Name	R/W	Default	Description
7	GPIO47_VAL	R/W	1	0: GPIO47 outputs 0 when in output mode. 1: GPIO47 outputs 1 when in output mode.
6	GPIO46_VAL	R/W	1	0: GPIO46 outputs 0 when in output mode. 1: GPIO46 outputs 1 when in output mode.
5	GPIO45_VAL	R/W	1	0: GPIO45 outputs 0 when in output mode. 1: GPIO45 outputs 1 when in output mode.
4	GPIO44_VAL	R/W	1	0: GPIO44 outputs 0 when in output mode. 1: GPIO44 outputs 1 when in output mode.
3	GPIO43_VAL	R/W	1	0: GPIO43 outputs 0 when in output mode. 1: GPIO43 outputs 1 when in output mode.

2	GPIO42_VAL	R/W	1	0: GPIO42 outputs 0 when in output mode. 1: GPIO42 outputs 1 when in output mode.
1	GPIO41_VAL	R/W	1	0: GPIO41 outputs 0 when in output mode. 1: GPIO41 outputs 1 when in output mode.
0	GPIO40_VAL	R/W	1	0: GPIO40 outputs 0 when in output mode. 1: GPIO40 outputs 1 when in output mode.

6.20.25 GPIO4 Pin Status Register — Index B2h

Bit	Name	R/W	Default	Description
7	GPIO47_IN	R	-	The pin status of PS_ON#/GPIO47.
6	GPIO46_IN	R	-	The pin status of PSOUT#/GPIO46
5	GPIO45_IN	R	-	The pin status of PSIN#/GPIO45
4	GPIO44_IN	R	-	The pin status of ATXPG_IN/GPIO44
3	GPIO43_IN	R	-	The pin status of IRRX/GPIO43.
2	GPIO42_IN	R	-	The pin status of IRTX/GPIO42.
1	GPIO41_IN	R	-	The pin status of FANCTL3/GPIO41.
0	GPIO40_IN	R	-	The pin status of FANIN3/GPIO40.

6.20.26 GPIO4 Drive Enable Register — Index B3h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved
3	GPIO43_DRV_EN	R/W	0	0: GPIO43 is open drain in output mode. 1: GPIO43 is push pull in output mode.
2	GPIO42_DRV_EN	R/W	0	0: GPIO42 is open drain in output mode. 1: GPIO42 is push pull in output mode.
1	GPIO41_DRV_EN	R/W	0	0: GPIO41 is open drain in output mode. 1: GPIO41 is push pull in output mode.
0	GPIO40_DRV_EN	R/W	0	0: GPIO40 is open drain in output mode. 1: GPIO40 is push pull in output mode.

6.20.27 GPIO4 PME Enable Register — Index B4h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved
3	GPIO43_PME_EN	R/W	0	When GPIO43_EVENT_STS is 1 and GPIO43_PME_EN is set to 1, a GPIO PME event will be generated.
2	GPIO42_PME_EN	R/W	0	When GPIO42_EVENT_STS is 1 and GPIO42_PME_EN is set to 1, a GPIO PME event will be generated.
1	GPIO41_PME_EN	R/W	0	When GPIO41_EVENT_STS is 1 and GPIO41_PME_EN is set to 1, a GPIO PME event will be generated.
0	GPIO40_PME_EN	R/W	0	When GPIO40_EVENT_STS is 1 and GPIO40_PME_EN is set to 1, a GPIO PME event will be generated.

6.20.28 GPIO4 Input Detection Select Register — Index B5h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved
3	GPIO43_DET_SEL	R/W	0	When GPIO43 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
2	GPIO42_DET_SEL	R/W	0	When GPIO42 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
1	GPIO41_DET_SEL	R/W	0	When GPIO41 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
0	GPIO40_DET_SEL	R/W	0	When GPIO40 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge

6.20.29 GPIO4 Event Status Register — Index B6h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved
3	GPIO43_ EVENT_STS	R/W	-	When GPIO43 is in input mode and a GPIO43 input is detected according to CRB5[3], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
2	GPIO42_ EVENT_STS	R/W	-	When GPIO42 is in input mode and a GPIO42 input is detected according to CRB5[2], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
1	GPIO41_ EVENT_STS	R/W	-	When GPIO41 is in input mode and a GPIO41 input is detected according to CRB5[1], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
0	GPIO40_ EVENT_STS	R/W	-	When GPIO40 is in input mode and a GPIO40 input is detected according to CRB5[0], this bit will be set to 1. Write a 1 to this bit will clear it to 0.

6.20.30 GPIO5 Output Enable Register — Index A0h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO54_OE	R/W	0	0: GPIO54 is in input mode. 1: GPIO54 is in output mode.
3	GPIO53_OE	R/W	0	0: GPIO53 is in input mode. 1: GPIO53 is in output mode.
2	GPIO52_OE	R/W	0	0: GPIO52 is in input mode. 1: GPIO52 is in output mode.

1	GPIO51_OE	R/W	0	0: GPIO51 is in input mode. 1: GPIO51 is in output mode.
0	GPIO50_OE	R/W	0	0: GPIO50 is in input mode. 1: GPIO50 is in output mode.

6.20.31 GPIO5 Output Data Register — Index A1h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO54_VAL	R/W	1	0: GPIO54 outputs 0 when in output mode. 1: GPIO54 outputs 1 when in output mode.
3	GPIO53_VAL	R/W	1	0: GPIO53 outputs 0 when in output mode. 1: GPIO53 outputs 1 when in output mode.
2	GPIO52_VAL	R/W	1	0: GPIO52 outputs 0 when in output mode. 1: GPIO52 outputs 1 when in output mode.
1	GPIO51_VAL	R/W	1	0: GPIO51 outputs 0 when in output mode. 1: GPIO51 outputs 1 when in output mode.
0	GPIO50_VAL	R/W	1	0: GPIO50 outputs 0 when in output mode. 1: GPIO50 outputs 1 when in output mode.

6.20.32 GPIO5 Pin Status Register — Index A2h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO54_IN	R	-	The pin status of DSKCHG#/GPIO54.
3	GPIO53_IN	R	-	The pin status of WPT#/GPIO53.
2	GPIO52_IN	R	-	The pin status of INDEX#/GPIO52.
1	GPIO51_IN	R	-	The pin status of TRK0#/GPIO51.
0	GPIO50_IN	R	-	The pin status of RDDATA#/GPIO50.

6.20.33 GPIO5 PME Enable Register — Index A4h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	GPIO54_PME_EN	R/W	0	When GPIO54_EVENT_STS is 1 and GPIO54_PME_EN is set to 1, a GPIO PME event will be generated.
3	GPIO53_PME_EN	R/W	0	When GPIO53_EVENT_STS is 1 and GPIO53_PME_EN is set to 1, a GPIO PME event will be generated.
2	GPIO52_PME_EN	R/W	0	When GPIO52_EVENT_STS is 1 and GPIO52_PME_EN is set to 1, a GPIO PME event will be generated.
1	GPIO51_PME_EN	R/W	0	When GPIO51_EVENT_STS is 1 and GPIO51_PME_EN is set to 1, a GPIO PME event will be generated.
0	GPIO50_PME_EN	R/W	0	When GPIO50_EVENT_STS is 1 and GPIO50_PME_EN is set to 1, a GPIO PME event will be generated.

6.20.34 GPIO5 Input Detection Select Register — Index A5h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	GPIO54_DET_SEL	R/W	0	When GPIO54 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
3	GPIO53_DET_SEL	R/W	0	When GPIO53 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
2	GPIO52_DET_SEL	R/W	0	When GPIO52 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
1	GPIO51_DET_SEL	R/W	0	When GPIO51 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
0	GPIO50_DET_SEL	R/W	0	When GPIO50 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge

6.20.35 GPIO5 Event Status Register — Index A6h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	GPIO54_ EVENT_STS	R/W	-	When GPIO54 is in input mode and a GPIO54 input is detected according to CRA5[4], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
3	GPIO53_ EVENT_STS	R/W	-	When GPIO53 is in input mode and a GPIO53 input is detected according to CRA5[3], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
2	GPIO52_ EVENT_STS	R/W	-	When GPIO52 is in input mode and a GPIO52 input is detected according to CRB5[2], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
1	GPIO51_ EVENT_STS	R/W	-	When GPIO51 is in input mode and a GPIO51 input is detected according to CRB5[1], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
0	GPIO50_ EVENT_STS	R/W	-	When GPIO50 is in input mode and a GPIO50 input is detected according to CRB5[0], this bit will be set to 1. Write a 1 to this bit will clear it to 0.

6.20.36 GPIO5 KBC Emulation Control Register 1— Index A9h

Bit	Name	R/W	Default	Description
7-6	DELAY_TIME	R/W	00	The delay time for repeat make code. 00: 500ms ~ 750ms. 01: 750ms ~ 1000ms. 10: 1000ms ~ 1250ms. 11: 1250ms ~ 1500ms.
5-4	REP_TIME	R/W	00	The make code repeat time select. 00: 50ms. 01: 100ms. 10: 250ms. 11: 500ms.
3	Reserved	-	-	Reserved.
2-0	MAKE_CODE_SEL	R/W	000	Make code select. Select which make code to be accessed. 000: GPIO50 make code. 001: GPIO51 make code. 010: GPIO52 make code. 011: GPIO53 make code. 100: GPIO54 make code. This changes the content of GP_MAKE_CODE register (CRAB).

6.20.37 GPIO5 KBC Make Code Register — Index ABh

Bit	Name	R/W	Default	Description
7-0	GP_MAKE_CODE	R/W	00h	This byte is the make code for GPIO5 KBC emulation. The break code will be GP_MAKE_CODE + 0x80.

6.20.38 GPIO5 KBC Prefix Code Register — Index ACh

Bit	Name	R/W	Default	Description
7-0	GP_PRE_CODE	R/W	E0h	This byte is the prefix code for GPIO5 KBC emulation if PRE_CODE_EN is set.

6.20.39 GPIO5 KBC Emulation Status Register 1— Index ADh

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GP54_BRK_STS	R/W	0	Break code status of GPIO54. It will be set if GPIO54 is released (rising edge). Write “1” to clear this bit.
3	GP53_BRK_STS	R/W	0	Break code status of GPIO53. It will be set if GPIO53 is released (rising edge). Write “1” to clear this bit.
2	GP52_BRK_STS	R/W	0	Break code status of GPIO52. It will be set if GPIO52 is released (rising edge). Write “1” to clear this bit.
1	GP51_BRK_STS	R/W	0	Break code status of GPIO51. It will be set if GPIO51 is released (rising edge). Write “1” to clear this bit.
0	GP50_BRK_STS	R/W	0	Break code status of GPIO50. It will be set if GPIO50 is released (rising edge). Write “1” to clear this bit.

6.20.40 GPIO5 KBC Emulation Status Register 2— Index AEh

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GP54_MAKE_STS	R/W	0	Make code status of GPIO54. It will be set if GPIO54 is pressed (falling edge). Write “1” to clear this bit.
3	GP53_MAKE_STS	R/W	0	Make code status of GPIO53. It will be set if GPIO53 is pressed (falling edge). Write “1” to clear this bit.
2	GP52_MAKE_STS	R/W	0	Make code status of GPIO52. It will be set if GPIO52 is pressed (falling edge). Write “1” to clear this bit.
1	GP51_MAKE_STS	R/W	0	Make code status of GPIO51. It will be set if GPIO51 is pressed (falling edge). Write “1” to clear this bit.
0	GP50_MAKE_STS	R/W	0	Make code status of GPIO50. It will be set if GPIO50 is pressed (falling edge). Write “1” to clear this bit.

6.20.41 GPIO5 KBC Emulation Control Register 2— Index AFh

Bit	Name	R/W	Default	Description
7	GP_KBC_EN	R/W	0	0: Disable GPIO5 KBC emulation function. 1: Enable GPIO5 KBC emulation function.
6	PRE_CODE_EN	R/W	0	0: One byte is sent when GPIO5 event occurs. 1: Two bytes are sent when GPIO5 event occurs. The prefix code is defined by GP_PRE_CODE.
5	Reserved	-	-	Reserved.
4	GP54_EVENT_EN	R/W	0	0: Disable GPIO54 event detection. 1: Enable GPIO54 event detection.
3	GP53_EVENT_EN	R/W	0	0: Disable GPIO53 event detection. 1: Enable GPIO53 event detection.
2	GP52_EVENT_EN	R/W	0	0: Disable GPIO52 event detection. 1: Enable GPIO52 event detection.
1	GP51_EVENT_EN	R/W	0	0: Disable GPIO51 event detection. 1: Enable GPIO51 event detection.
0	GP50_EVENT_EN	R/W	0	0: Disable GPIO50 event detection. 1: Enable GPIO50 event detection.

6.20.42 GPIO6 Output Enable Register — Index 90h

Bit	Name	R/W	Default	Description
7	GPIO67_OE	R/W	0	0: GPIO67 is in input mode. 1: GPIO67 is in output mode.
6	GPIO66_OE	R/W	0	0: GPIO66 is in input mode. 1: GPIO66 is in output mode.
5	GPIO65_OE	R/W	0	0: GPIO65 is in input mode. 1: GPIO65 is in output mode.
4	GPIO64_OE	R/W	0	0: GPIO64 is in input mode. 1: GPIO64 is in output mode.
3	GPIO63_OE	R/W	0	0: GPIO63 is in input mode. 1: GPIO63 is in output mode.

2	GPIO62_OE	R/W	0	0: GPIO62 is in input mode. 1: GPIO62 is in output mode.
1	GPIO61_OE	R/W	0	0: GPIO61 is in input mode. 1: GPIO61 is in output mode.
0	GPIO60_OE	R/W	0	0: GPIO60 is in input mode. 1: GPIO60 is in output mode.

6.20.43 GPIO6 Output Data Register — Index 91h

Bit	Name	R/W	Default	Description
7	GPIO67_VAL	R/W	1	0: GPIO67 outputs 0 when in output mode. 1: GPIO67 outputs 1 when in output mode.
6	GPIO66_VAL	R/W	1	0: GPIO66 outputs 0 when in output mode. 1: GPIO66 outputs 1 when in output mode.
5	GPIO65_VAL	R/W	1	0: GPIO65 outputs 0 when in output mode. 1: GPIO65 outputs 1 when in output mode.
4	GPIO64_VAL	R/W	1	0: GPIO64 outputs 0 when in output mode. 1: GPIO64 outputs 1 when in output mode.
3	GPIO63_VAL	R/W	1	0: GPIO63 outputs 0 when in output mode. 1: GPIO63 outputs 1 when in output mode.
2	GPIO62_VAL	R/W	1	0: GPIO62 outputs 0 when in output mode. 1: GPIO62 outputs 1 when in output mode.
1	GPIO61_VAL	R/W	1	0: GPIO61 outputs 0 when in output mode. 1: GPIO61 outputs 1 when in output mode.
0	GPIO60_VAL	R/W	1	0: GPIO60 outputs 0 when in output mode. 1: GPIO60 outputs 1 when in output mode.

6.20.44 GPIO6 Pin Status Register — Index 92h

Bit	Name	R/W	Default	Description
7	GPIO67_IN	R	-	The pin status of STB#/GPIO67.
6	GPIO66_IN	R	-	The pin status of AFD#/GPIO66.
5	GPIO65_IN	R	-	The pin status of ERR#/GPIO65.
4	GPIO64_IN	R	-	The pin status of INIT#/GPIO64.
3	GPIO63_IN	R	-	The pin status of ACK#/GPIO63.
2	GPIO62_IN	R	-	The pin status of BUSY/GPIO62.
1	GPIO61_IN	R	-	The pin status of PE/GPIO61.
0	GPIO60_IN	R	-	The pin status of SLCT/GPIO60.

6.20.45 GPIO6 Drive Enable Register — Index 93h

Bit	Name	R/W	Default	Description
7	GPIO67_DRV_EN	R/W	0	0: GPIO67 is open drain in output mode. 1: GPIO67 is push pull in output mode.
6	GPIO66_DRV_EN	R/W	0	0: GPIO66 is open drain in output mode. 1: GPIO66 is push pull in output mode.

5	GPIO65_DRV_EN	R/W	0	0: GPIO65 is open drain in output mode. 1: GPIO65 is push pull in output mode.
4	GPIO64_DRV_EN	R/W	0	0: GPIO64 is open drain in output mode. 1: GPIO64 is push pull in output mode.
3	GPIO63_DRV_EN	R/W	0	0: GPIO63 is open drain in output mode. 1: GPIO63 is push pull in output mode.
2	GPIO62_DRV_EN	R/W	0	0: GPIO62 is open drain in output mode. 1: GPIO62 is push pull in output mode.
1	GPIO61_DRV_EN	R/W	0	0: GPIO61 is open drain in output mode. 1: GPIO61 is push pull in output mode.
0	GPIO60_DRV_EN	R/W	0	0: GPIO60 is open drain in output mode. 1: GPIO60 is push pull in output mode.

6.20.46 GPIO7 Output Enable Register — Index 80h

Bit	Name	R/W	Default	Description
7	GPIO77_OE	R/W	0	0: GPIO77 is in input mode. 1: GPIO77 is in output mode.
6	GPIO76_OE	R/W	0	0: GPIO76 is in input mode. 1: GPIO76 is in output mode.
5	GPIO75_OE	R/W	0	0: GPIO75 is in input mode. 1: GPIO75 is in output mode.
4	GPIO74_OE	R/W	0	0: GPIO74 is in input mode. 1: GPIO74 is in output mode.
3	GPIO73_OE	R/W	0	0: GPIO73 is in input mode. 1: GPIO73 is in output mode.
2	GPIO72_OE	R/W	0	0: GPIO72 is in input mode. 1: GPIO72 is in output mode.
1	GPIO71_OE	R/W	0	0: GPIO71 is in input mode. 1: GPIO71 is in output mode.
0	GPIO70_OE	R/W	0	0: GPIO70 is in input mode. 1: GPIO70 is in output mode.

6.20.47 GPIO7 Output Data Register — Index 91h

Bit	Name	R/W	Default	Description
7	GPIO77_VAL	R/W	1	0: GPIO77 outputs 0 when in output mode. 1: GPIO77 outputs 1 when in output mode.
6	GPIO76_VAL	R/W	1	0: GPIO76 outputs 0 when in output mode. 1: GPIO76 outputs 1 when in output mode.
5	GPIO75_VAL	R/W	1	0: GPIO75 outputs 0 when in output mode. 1: GPIO75 outputs 1 when in output mode.
4	GPIO74_VAL	R/W	1	0: GPIO74 outputs 0 when in output mode. 1: GPIO74 outputs 1 when in output mode.
3	GPIO73_VAL	R/W	1	0: GPIO73 outputs 0 when in output mode. 1: GPIO73 outputs 1 when in output mode.
2	GPIO72_VAL	R/W	1	0: GPIO72 outputs 0 when in output mode. 1: GPIO72 outputs 1 when in output mode.

1	GPIO71_VAL	R/W	1	0: GPIO71 outputs 0 when in output mode. 1: GPIO71 outputs 1 when in output mode.
0	GPIO70_VAL	R/W	1	0: GPIO70 outputs 0 when in output mode. 1: GPIO70 outputs 1 when in output mode.

6.20.48 GPIO7 Pin Status Register — Index 92h

Bit	Name	R/W	Default	Description
7	GPIO77_IN	R	-	The pin status of PD7/GPIO77.
6	GPIO76_IN	R	-	The pin status of PD6/GPIO76.
5	GPIO75_IN	R	-	The pin status of PD5/GPIO75.
4	GPIO74_IN	R	-	The pin status of PD4/GPIO74.
3	GPIO73_IN	R	-	The pin status of PD3/GPIO73.
2	GPIO72_IN	R	-	The pin status of PD2/GPIO72.
1	GPIO71_IN	R	-	The pin status of PD1/GPIO71.
0	GPIO70_IN	R	-	The pin status of PD0/GPIO70.

6.20.49 GPIO7 Drive Enable Register — Index 93h

Bit	Name	R/W	Default	Description
7	GPIO77_DRV_EN	R/W	0	0: GPIO77 is open drain in output mode. 1: GPIO77 is push pull in output mode.
6	GPIO76_DRV_EN	R/W	0	0: GPIO76 is open drain in output mode. 1: GPIO76 is push pull in output mode.
5	GPIO75_DRV_EN	R/W	0	0: GPIO75 is open drain in output mode. 1: GPIO75 is push pull in output mode.
4	GPIO74_DRV_EN	R/W	0	0: GPIO74 is open drain in output mode. 1: GPIO74 is push pull in output mode.
3	GPIO73_DRV_EN	R/W	0	0: GPIO73 is open drain in output mode. 1: GPIO73 is push pull in output mode.
2	GPIO72_DRV_EN	R/W	0	0: GPIO72 is open drain in output mode. 1: GPIO72 is push pull in output mode.
1	GPIO71_DRV_EN	R/W	0	0: GPIO71 is open drain in output mode. 1: GPIO71 is push pull in output mode.
0	GPIO70_DRV_EN	R/W	0	0: GPIO70 is open drain in output mode. 1: GPIO70 is push pull in output mode.

6.21 Watch Dog Timer Registers (CR07)

6.21.1 Configuration Register — Index F0h (Offset 00h)

(* Cleared by Slotocc# and watch dog timeout)

Bit	Name	R/W	Default	Description
7	WDOUT_EN	R/W	-	This bit is decided by RTS1# power-on trapping. If this bit is set to 1 and watchdog timeout event occurs, WDTRST# output is enabled.
6-1	Reserved	-	-	Reserved
0	WD_RST_EN	R/W	1	0: Disable WDT to reset the VID register marked with *. 1: Enable WDT to reset the VID register marked with *.

6.21.2 Serial Key Data Register 1 — Index F2h (Offset 02h)

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	KEY_OK	R	1	This bit is 1 represents that the serial key is entered correctly.
5-0	Reserved	-	-	Reserved

6.21.3 Serial Key Data Register 2 — Index F3h (Offset 03h)

Bit	Name	R/W	Default	Description
7-0	KEY_DATA	R/W	F3h	Write serial data to this register correctly, the KEY_OK bit will be set to 1. Hence, users are able to write key protected registers. The sequence to enable KEY_OK is 0x32, 0x5D, 0x42, 0xAC. When KEY_OK is set, write this register 0x35 will clear KEY_OK.

6.21.4 Reserved — Index F4h (Offset 04h)

Bit	Name	R/W	Default	Description
7-0	Reserved	-	-	Reserved

6.21.5 Watchdog Timer Configuration Register 1— Index F5h (Offset 05h)

Bit	Name	R/W	Default	Description
7	WDT_CLK_SEL	R	0	Select the WDT clock source. 0: The clock source is from CLKIN. (powered by VDD and is accurate)\ 1: The clock source is from internal 500KHz (powered by VSB3V and 20% tolerance).
6	WDTMOUT_STS	R/W	0	If watchdog timeout event occurs, this bit will be set to 1. Write a 1 to this bit will clear it to 0.

5	WD_EN	R/W	-	This bit is decided by RTS1# power-on trapping. If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	0	Select output mode (0: level, 1: pulse) of RSTOUT# by setting this bit.
3	WD_UNIT	R/W	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	0	Select output polarity of RSTOUT# (1: high active, 0: low active) by setting this bit.
1:0	WD_PSWIDTH	R/W	0	Select output pulse width of RSTOUT# 0: 750 us 1: 18 ms 2: 93 ms 3: 3.75 sec

6.21.6 Watchdog Timer Configuration Register 2 — Index F6h (Offset 06h)

Bit	Name	R/W	Default	Description
7:0	WD_TIME	R/W	0A	Time of watchdog timer

6.21.7 WDT PME Register — Index F7h (Offset 07h)

Bit	Name	R/W	Default	Description
7	WDT_PME	R	0	WDT PME real time status.
6	WDT_PME_EN	R/W	0	0: Disable WDT PME. 1: Enable WDT PME.
6	WDT_PME_ST	R/W	0	0: No WDT PME occurred. 1: WDT PME occurred. The WDT PME is occurred one unit before WDT timeout.
4-1	Reserved	R	0	Reserved
0	CPU_CHANGE	R/WC	-	This bit will be set at SLOTOCC# rising edge. Internal 1us de-bounce circuit is implemented. Write “1” to this bit will clear the status.(This bit is powered by VBAT.)

6.22 CIR Registers (CR08)

Configuration Registers

6.22.1 CIR Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	0	Reserved
0	CIR_EN	R/W	0	0: disable CIR 1: enable CIR

6.22.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of CIR base address.

6.22.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	00h	The LSB of CIR base address.

6.22.4 CIRIRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELCIRIRQ	R/W	0h	Select the IRQ channel for CIR interrupt.

Device Registers

6.22.5 CIR Status Register — Index 00h

Bit	Name	R/W	Default	Description
7	CIR_IRQ_EN	R/W	0	CIR IRQ function enable
6-4	Reserved	R	0	Reserved
3	TX_FINISH	R/W	0	CIR transmittion finish status. Write 1 clear.
2	TX_UNDERRUN	R/W	0	CIR transmitttion underrun status. Write 1 clear.
1	RX_TIMEOUT	R/W	0	CIR receiver timeout status. Write 1 clear.
0	RX_RECEIVE	R/W	0	CIR receiver receives data status. Write 1 clear.

6.22.6 CIR RX Data Register — Index 01h

Bit	Name	R/W	Default	Description
7-0	RX_DATA	R	-	CIR received data is read from here.

6.22.7 CIR TX Control Register — Index 02h

Bit	Name	R/W	Default	Description
7	TX_START	R/W	0	Set 1 to start CIR TX transmittion and will be auto cleared if transmittion is finished.
6	TX_END	R/W	0	Set 1 to indicate that all TX data has been written to CIR TX FIFO.
5-0	Reserved	-	-	Reserved

6.22.8 CIR TX Data Register — Index 03h

Bit	Name	R/W	Default	Description
7-0	TX_DATA	R/W	-	The transmittion data should be written to TX_DATA.

6.22.9 CIR Control Register — Index 04h

Bit	Name	R/W	Default	Description
7-0	CIR_CMD	R/W	0	Host writes command to CIR.

6.23 PME, ACPI, and ERP Power Saving Registers (CR0A)

6.23.1 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	PME_EN	R/W	0	0: disable PME. 1: enable PME.

6.23.2 ERP Enable Register — Index E0h

Bit	Name	R/W	Default	Description
7	EUP_EN	R/W	0	0 : disable ERP function 1: enable ERP function
6	S3_BACK	R/W	0	This bit will set “1” when system is back from S3 state.
5-2	Reserved	-	-	Reserved
1	RING_PME_EN	R/W	0	RING1 PME event enable. 0: disable RING1 PME event. 1: enable RING1 PME event, when RING1 falling edge detect
0	RING_PSOUT_EN	R/W	0	RING1 PSOUT event enable. 0: disable RING1 PSOUT event. 1: enable RING1 PSOUT event, when RING1 falling edge detect

6.23.3 ERP control register — Index E1h

Bit	Name	R/W	Default	Description
7-6	Boot_Mode	R/W	11	Write these two bits to select Boot Mode for Always Off/ Always On/ Keep Last State. 00:Always Off 11:Support Always On and Keep Last State 10:Reserved 01:Reserved
5	S3_ ERP_CTRL1#_DIS	R/W	0	If clear to “0” ERP_CTRL1# will output Low when S3 state. Else If set to “1” ERP_CTRL1# will output High when S3 state.
4	S3 _ ERP_CTRL0#_DIS	R/W	0	If clear to “0” ERP_CTRL0# will output Low when S3 state. Else If set to “1” ERP_CTRL0# will output High when S3 state.
3	S5 _ ERP_CTRL1#_DIS	R/W	1	If clear to “0” ERP_CTRL1# will output Low when S5 state. Else If set to “1” ERP_CTRL1# will output High when S5 state.
2	S5 _ ERP_CTRL0#_DIS	R/W	1	If clear to “0” ERP_CTRL0# will output Low when S5 state. Else If set to “1” ERP_CTRL0# will output High when S5 state.
1	AC_ ERP_CTRL1#_DIS	R/W	0	If clear to “0” ERP_CTRL1# will output Low when after AC lost. Else If set to “1” ERP_CTRL1# will output High when after AC lost.
0	AC_ ERP_CTRL0#_DIS	R/W	0	If clear to “0” ERP_CTRL0# will output Low when after AC lost. Else If set to “1” ERP_CTRL0# will output High when after AC lost.

6.23.4 ERP control register — Index E2h

Bit	Name	R/W	Default	Description
7	AC_LOST	R	-	This bit is AC lost status and writes 1 to this bit will clear it.
6	Reserved	R/W	0	Reserved
5	VSB_CTRL_EN[1]	R/W	1'b0	0: Disable ERP_CTRL1# assert RSMRST low 1: Enable ERP_CTRL1# assert RSMRST low
4	VSB_CTRL_EN[0]	R/W	1'b0	0: Disable ERP_CTRL0# assert RSMRST low 1: Enable ERP_CTRL0# assert RSMRST low
3-2	Reserved	R/W	0	Reserved
1	RSMRST_DET_5V_N	R/W	0	Device detects VSB5V power ok (4.4V) and VSB3V_IN become high, and after ~50ms de-bounce time RSMRST will become high. But when user set this bit to 1. RSMRST will not check VSB5V power ok.
0	Reserved	R	-	Reserved

6.23.5 ERP PSIN deb-register — Index E3h

Bit	Name	R/W	Default	Description
7-0	PS_DEB_TIME	R/W	0x13	PS_IN pin input de-bounce time default is ~20mSec

6.23.6 ERP RSMRST deb-register — Index E4h

Bit	Name	R/W	Default	Description
7-0	RSMRST_DEB_TIME	R/W	0x09	RSMRST internal de-bounce time default is ~10mSec

6.23.7 ERP PSOUT deb-register — Index E5h

Bit	Name	R/W	Default	Description
7-0	PS_OUT_PULSE_W	R/W	0xC7	PS_OUT_OUT output Pulse width default is ~200mSec low pulse

6.23.8 ERP PSON deb-register — Index E6h

Bit	Name	R/W	Default	Description
7-0	PS_ON_DEB_TIME	R/W	0x09	PSON_IN pin input de-bounce time default is 10mSec

6.23.9 ERP S5 Delay Register — Index E7h

Bit	Name	R/W	Default	Description
7-0	S5_DEL_TIME	R/W	0x63	S5 to deep S5 state delay time. The unit of this byte is 6.4 s.

6.23.10 Wakeup Enable register — Index E8h

Bit	Name	R/W	Default	Description
7	RI2_WAKEUP_EN	R/W	0	Set this bit to enable RI2# event to wakeup system.
6	CIR_WAKEUP_EN	R/W	0	Set this bit to enable CIR event to wakeup system.
5	RI1_WAKEUP_EN	R/W	0	Set this bit to enable RI1# event to wakeup system.
4	RING_WAKEUP_EN	R/W	1	Set this bit to enable EVENT_IN0# event to wakeup system.

3	GP_WAKEUP_EN	R/W	0	Set this bit to enable GPIO event to wakeup system.
2	TMOUT_WAKEUP_EN	R/W	0	Set this bit to enable Timeout event to wakeup system.
1	MO_WAKEUP_EN	R/W	0	Set this bit to enable Mouse event to wakeup system.
0	KB_WAKEUP_EN	R/W	0	Set this bit to enable Keyboard event to wakeup system.

6.23.11 ERP S3 Delay Register — Index E9h

Bit	Name	R/W	Default	Description
7-0	S3_DEL_TIME	R/W	0x0F	S3 to deep S3 state delay time. The unit of this byte is 64ms.

6.23.12 ERP Mode Select register — Index ECh

Bit	Name	R/W	Default	Description
7-6	ERP_MODE	R/W	0	00: Fintek G3' mode. 01: Intel DSW + Fintek G3` mode. 10: Reserved. 11: Intel DSW mode.
5	DPWROK_CTRL_EN	R/W	0	Set "1" to enable DPWROK reset by ERP_CTRL1#.
4-0	Reserved	R	-	Reserved

6.23.13 ERP WDT Control register — Index EDh

Bit	Name	R/W	Default	Description
7-5	Reserved	R	-	Reserved
4	ERP_WDTMOUT	R	-	ERP WDT timeout status.
3-2	Reserved	R	-	Reserved
1	WD_UNIT	R/W	0	ERP WDT unit. It is the time unit of ERP_WD_TIME. 0: 1sec. 1: 60 sec.
0	WD_EN	R/W	0	Set "1" to enable ERP WDT. Auto clear if timeout occurs.

6.23.14 ERP WDT Timer — Index EEh

Bit	Name	R/W	Default	Description
7-0	ERP_WD_TIME	R/W	0	Time of ERP watchdog timer.

6.23.15 PME Event Enable Register 1— Index F0h

Bit	Name	R/W	Default	Description
7	WDT_PME_EN	R/W	0	WDT PME event enable. 0: disable WDT PME event. 1: enable WDT PME event.
6	MO_PME_EN	R/W	0	Mouse PME event enable. 0: disable mouse PME event. 1: enable mouse PME event.
5	KB_PME_EN	R/W	0	Keyboard PME event enable. 0: disable keyboard PME event. 1: enable keyboard PME event.

4	HM_PME_EN	R/W	0	Hardware monitor PME event enable. 0: disable hardware monitor PME event. 1: enable hardware monitor PME event.
3	PRT_PME_EN	R/W	0	Parallel port PME event enable. 0: disable parallel port PME event. 1: enable parallel port PME event.
2	UR2_PME_EN	R/W	0	UART 2 PME event enable. 0: disable UART 2 PME event. 1: enable UART 2 PME event.
1	UR1_PME_EN	R/W	0	UART 1 PME event enable. 0: disable UART 1 PME event. 1: enable UART 1 PME event.
0	FDC_PME_EN	R/W	0	FDC PME event enable. 0: disable FDC PME event. 1: enable FDC PME event.

6.23.16 PME Event Status Register — Index F1h

Bit	Name	R/W	Default	Description
7	WDT_PME_ST	R/W	-	WDT PME event status. 0: WDT has no PME event. 1: WDT has a PME event to assert. Write 1 to clear to be ready for next PME event.
6	MO_PME_ST	R/W	-	Mouse PME event status. 0: Mouse has no PME event. 1: Mouse has a PME event to assert. Write 1 to clear to be ready for next PME event.
5	KB_PME_ST	R/W	-	Keyboard PME event status. 0: Keyboard has no PME event. 1: Keyboard has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	HM_PME_ST	R/W	-	Hardware monitor PME event status. 0: Hardware monitor has no PME event. 1: Hardware monitor has a PME event to assert. Write 1 to clear to be ready for next PME event.
3	PRT_PME_ST	R/W	-	Parallel port PME event status. 0: Parallel port has no PME event. 1: Parallel port has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	UR2_PME_ST	R/W	-	UART 2 PME event status. 0: UART 2 has no PME event. 1: UART 2 has a PME event to assert. Write 1 to clear to be ready for next PME event.
1	UR1_PME_ST	R/W	-	UART 1 PME event status. 0: UART 1 has no PME event. 1: UART 1 has a PME event to assert. Write 1 to clear to be ready for next PME event.

0	FDC_PME_ST	R/W	-	FDC PME event status. 0: FDC has no PME event. 1: FDC has a PME event to assert. Write 1 to clear to be ready for next PME event.

6.23.17 PME Event Enable Register 2 — Index F2h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	CIR_PME_EN	R/W	0	CIR PME event enable. 0: disable CIR PME event. 1: enable CIR PME event.
3	Reserved	-	-	Reserved
2	RI2_PME_EN	R/W	0	RI2# PME event enable. 0: disable RI2# PME event. 1: enable RI2# PME event.
1	RI1_PME_EN	R/W	0	RI1# PME event enable. 0: disable RI1# PME event. 1: enable RI1# PME event.
0	GP_PME_EN	R/W	0	GPIO PME event enable. 0: disable GPIO PME event. 1: enable GPIO PME event.

6.23.18 PME Event Status Register — Index F3h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	CIR_PME_ST	R/W	-	CIR PME event status. 0: CIR has no PME event. 1: CIR has a PME event to assert. Write 1 to clear to be ready for next PME event.
3	ERP_PME_ST	R/W	-	ERP PME event status. 0: ERP has no PME event. 1: ERP has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	RI2_PME_ST	R/W	-	RI2# PME event status. 0: RI2# has no PME event. 1: RI2# has a PME event to assert. Write 1 to clear to be ready for next PME event.
1	RI1_PME_ST	R/W	-	RI1# PME event status. 0: RI1# has no PME event. 1: RI1# has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	GP_PME_ST	R/W	-	GPIO PME event status. 0: GPIO has no PME event. 1: GPIO has a PME event to assert. Write 1 to clear to be ready for next PME event.

6.23.19 Keep Last State Select Register — Index F4h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	-
6	EN_CIRWAKEUP	R/W	0	Set one to enable CIR wakeup event asserted via PSOUT#.
5	EN_GPWAKEUP	R/W	0	Set one to enable GPIO wakeup event asserted via PSOUT#.
4	EN_KBWAKEUP	R/W	0	Set one to enable keyboard wakeup event asserted via PSOUT#.
3	EN_MOWAKEUP	R/W	0	Set one to enable mouse wakeup event asserted via PSOUT#.
2-1	PWRCTRL	R/W	11	The ACPI Control the PSON_N to always on or always off or keep last state 00 : Keep last state 10 : Always on 01 : Bypass mode. 11: Always off
0	VSB_PWR_LOSS	R/W	0	When VSB 3V comes, it will set to 1, and write 1 to clear it

6.23.20 VDDOK Delay Register — Index F5h (powered by VBAT)

Bit	Name	R/W	Default	Description
7-6	PWROK_DELAY	R/W	0	The additional PWROK delay. The unit is 75 ms. 00: no delay 01: 1X 10: 2X 11: 4X
5	RSTCON_EN	R/W	0	0: RSTCON# will assert via PWROK. 1: RSTCON# will assert via PCIRST4# and PCIRST5#.
4-3	VDD_DELAY	R/W	11	The PWROK delay timing from VDD3VOK by followed setting. The unit is 75 ms. 00 : 1X 01 : 2X 10 : 3X 11 : 4X
2	VINDB_EN	R/W	1	Enable the PCIRSTIN_N and ATXPWGD de-bounce.
1	PCIRST_DB_EN	R/W	0	Enable the LRESET_N de-bounce.
0	Reserved	R/W	0	Reserved

6.23.21 PCIRST Control Register — Index F6h

Bit	Name	R/W	Default	Description
7	S3_SEL	R/W	0	Select the KBC S3 state. 0: Enter S3 state when internal VDD3VOK signal de-asserted. 1: Enter S3 state when S3# is low or the TS3 register is set to 1.
6	PSON_DEL_EN	R/W	0	0: PSON# is the inverted of S3# signal. 1: PSON# will sink low only if the time after the last turn-off elapse at least 4 seconds.
5	Reserved	-	-	Reserved
4	PCIRST5_GATE	R/W	1	Write “0” to this bit will force PCIRST5# to sink low.
3	PCIRST4_GATE	R/W	1	Write “0” to this bit will force PCIRST4# to sink low.
2	PCIRST3_GATE	R/W	1	Write “0” to this bit will force PCIRST3# to sink low.

1	PCIRST2_GATE	R/W	1	Write “0” to this bit will force PCIRST2# to sink low.
0	PCIRST1_GATE	R/W	1	Write “0” to this bit will force PCIRST1# to sink low.

6.23.22 Power Sequence Control Register — Index F7h (powered by VBAT)

Bit	Name	R/W	Default	Description
7	VDIMM_S3_ON	R/W	1	0: TIMING_1 will low during S3 state. 1: TIMING_1 will be tri-state during S3 state.
6	VDDA_S3_ON	R/W	0	0: TIMING_2 will low during S3 state. 1: TIMING_2 will be tri-state during S3 state.
5	VCORE_S3_ON	R/W	0	0: TIMING_3 will low during S3 state. 1: TIMING_3 will be tri-state during S3 state.
4	VLDT_S3_ON	R/W	0	0: TIMING_4 will low during S3 state. 1: TIMING_4 will be tri-state during S3 state.
3	WDT_PWROK_EN	R/W	0	Set “1” to enable WDTRST# assert from PWROK pin.
2	S0P5_Gate#_TRI	R/W	1	0: S0P5_Gate# will sink low in S5 state. 1: S0P5_Gate# will be tri-state in S5 state.
1	PWR_ S3P5_Gate#_TRI	R/W	1	0: S3P5_Gate# will sink low in S5 state. 1: S3P5_Gate# will be tri-state in S5 state.
0	Reserved	R/W	0	Reserved

6.23.23 LED VCC Mode Select Register — Index F8h

Bit	Name	R/W	Default	Description
7	LED_INV_DIS	R/W	0	0: Default Invert signal 1: Invert disable
6	LED_VCC_DS3	R/W	0	0: Disable LED_VCC deep S3 mode. 1: Enable LED_VCC deep S3 mode. LED_VCC will output 0.25Hz clock with 75% duty when enter deep S3 state.
5-4	LED_VCC_S5_MODE	R/W	0	Select LED_VCC mode in S5 state. The mode is controlled by {LED_VCC_S5_ADD, LED_VCC_S5_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
3-2	LED_VCC_S3_MODE	R/W	0	Select LED_VCC mode in S3 state. The mode is controlled by {LED_VCC_S3_ADD, LED_VCC_S3_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.

1-0	LED_VCC_S0_MODE	R/W	0	Select LED_VCC mode in S0 state. The mode is controlled by {LED_VCC_S0_ADD, LED_VCC_S0_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.

6.23.24 LED VSB Mode Select Register — Index F9h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	LED_VSB_DS3	R/W	0	0: Disable LED_VSB deep S3 mode. 1: Enable LED_VSB deep S3 mode. LED_VSB will output 0.25Hz clock with 75% duty when enter deep S3 state.
5-4	LED_VSB_S5_MODE	R/W	0	Select LED_VSB mode in S5 state. The mode is controlled by {LED_VSB_S5_ADD, LED_VSB_S5_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
3-2	LED_VSB_S3_MODE	R/W	0	Select LED_VSB mode in S3 state. The mode is controlled by {LED_VSB_S3_ADD, LED_VSB_S3_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
1-0	LED_VSB_S0_MODE	R/W	0	Select LED_VSB mode in S0 state. The mode is controlled by {LED_VSB_S0_ADD, LED_VSB_S0_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.

6.23.25 LED Additional Mode Select Register — Index FAh

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	LED_VSB_S5_ADD	R/W	0	Select LED_VSB mode in S5 state. The mode is controlled by {LED_VSB_S5_ADD, LED_VSB_S5_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
5	LED_VSB_S3_ADD	R/W	0	Select LED_VSB mode in S3 state. The mode is controlled by {LED_VSB_S3_ADD, LED_VSB_S3_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
4	LED_VSB_S0_ADD	R/W	0	Select LED_VSB mode in S0 state. The mode is controlled by {LED_VSB_S0_ADD, LED_VSB_S0_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
3	Reserved	-	-	Reserved
2	LED_VCC_S5_ADD	R/W	0	Select LED_VCC mode in S5 state. The mode is controlled by {LED_VCC_S5_ADD, LED_VCC_S5_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.

1	LED_VCC_S3_ADD	R/W	0	Select LED_VCC mode in S3 state. The mode is controlled by {LED_VCC_S3_ADD, LED_VCC_S3_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
0	LED_VCC_S0_ADD	R/W	0	Select LED_VCC mode in S0 state. The mode is controlled by {LED_VCC_S0_ADD, LED_VCC_S0_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.

6.23.26 Intel DSW Delay Select Register — Index FCh

Bit	Name	R/W	Default	Description
7-4	Reserved	R/W	-	Reserved
3-0	DSW_DELAY	R/W	7h	This is the delay time for SUS_ACK# and SUS_WARN#. Time unit is 0.5s.

6.23.27 RI De-bounce Select Register — Index FEh

Bit	Name	R/W	Default	Description
7	WR_TRIM_EN	R/W	0	After entry key is enabled, write “1” to enable trim operation.
6	WR_KEY_EN	R/W	0	Enable CRFD for entry data.
5	Reserved	-	-	Reserved
4	CIR_VDD_S3	R/W	0	Write “1” to emulate a S3 state for CIR.
3-2	Reserved	-	-	Reserved
1-0	RI_DB_SEL	R/W	0	Select RI de-bounce time. 00: reserved. 01: 200us. 10: 2ms. 11: 20ms.

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.5	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may dversely affect the life and reliability of the device.

7.2 DC Characteristics

(Ta = 0° C to 70° C, 3VCC = 3.3V ± 10%, VSS = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Operating Voltage	VDD	3.0	3.3	3.6	V	
Battery Voltage	VBAT	2.4	3.3	3.6	V	
Operating Current	ICC		10		mA	3VCC=3.3V VBAT=3.3V
Idle State Current	ISTY		5		uA	3VCC=3.3V VBAT=3.3V
Battery Current	IBAT		4		uA	3VCC=3.3V VBAT=3.3V

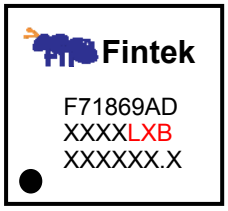
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
$I/O_{12st,5v}$-TTL level bi-directional pin with schmitt trigger, output with12 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/O_{16t,u47k}$-TTL level bi-directional pin with 16 mA source-sink capability, internal pull-up 47k ohms						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+16		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OOD_{12t}-TTL level bi-directional pin, Output pin with 12mA source-sink capability, and can programming to open-drain function.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/OOD_{12t,5v}$-TTL level bi-directional pin, Output pin with 12mA source-sink capability, and can programming to open-drain function, 5v tolerance.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V

Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/OOD_{8st,5v}$-TTL level bi-directional pin and schmitt triggrt, Open-drain output with 8mA source-sink capability, 5v tolerance.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-8	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+8		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/OOD_{12st,5v}$-TTL level bi-directional pin and schmitt triggrt, Open-drain output with 12mA source-sink capability, 5v tolerance.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/OOD_{24st,5v}$-TTL level bi-directional pin and schmitt triggrt, Open-drain output with 24mA source-sink capability, 5v tolerance.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-24	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+24		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
IN_{st} - TTL level input pin with schmitt trigger						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{t,5v}$ - TTL level input pin with 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{st,5v}$ - TTL level input pin with schmitt trigger, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{st-u47k}$ - TTL level input pin with schmitt trigger, internal pull-up 47k ohms						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{st,lv}$ - TTL level input pin with schmitt trigger, low level.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V

OD_{12}-Open-drain output with12 mA sink capability.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
$OD_{12,5v}$-Open-drain output with12 mA sink capability, 5V tolerance.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
$OD_{14,5v}$-Open-drain output with14 mA sink capability, 5V tolerance.						
Output Low Current	IOL		-14		mA	VOL = 0.4V
$OD_{24,5v}$-Open-drain output with24 mA sink capability, 5V tolerance.						
Output Low Current	IOL		-24		mA	VOL = 0.4V
$OD_{12,u10k,5v}$-Open-drain output with 12 mA sink capability, pull-up 10k ohms, 5V tolerance.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
$OD_{16,u10k,5v}$-Open-drain output with 16 mA sink capability, pull-up 10k ohms, 5V tolerance.						
Output Low Current	IOL		-16		mA	VOL = 0.4V
$O_{8t,u47,5v}$- TTL level Output pin with 8 mA source-sink capability, pull-up 47k ohms, 5V tolerance.						
Output High Current	IOH	+6	+8		mA	VOH = 2.4V
O_{12}- Output pin with 12 mA source-sink capability.						
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
O_{16}- Output pin with 16 mA source-sink capability.						
Output High Current	IOH		+16		mA	VOH = 2.4V
O_{18}- Output pin with 18 mA source-sink capability.						
Output High Current	IOH		+18		mA	VOH = 2.4V
O_{20}- Output pin with 20 mA source-sink capability.						
Output High Current	IOH		+20		mA	VOH = 2.4V
O_{30}- Output pin with 30 mA source-sink capability.						
Output High Current	IOH	+26	+30		mA	VOH = 2.4V
$O_{12\text{-}5v}$- Output pin with 12 mA source-sink capability, 5V tolerance.						
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
$I_{LV}/O_{D8\text{-}s1}$ - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.). Output with 8mA drive and 1mA sink capability.						
Input Low Voltage	VIL			0.6	V	
Input High Voltage	VIH	0.9			V	
Output High Current	IOH		+8		mA	VOH = 1.0V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
I/$OD_{12st,5v}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with12 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/$OD_{14st,5v}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with 16 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+14		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/$OD_{16st,5v}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with 16 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+16		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V

8. Ordering Information

Part Number	Package Type	Production Flow
F71869AD	128-LQFP (Green Package)	Commercial, 0°C to +70°C



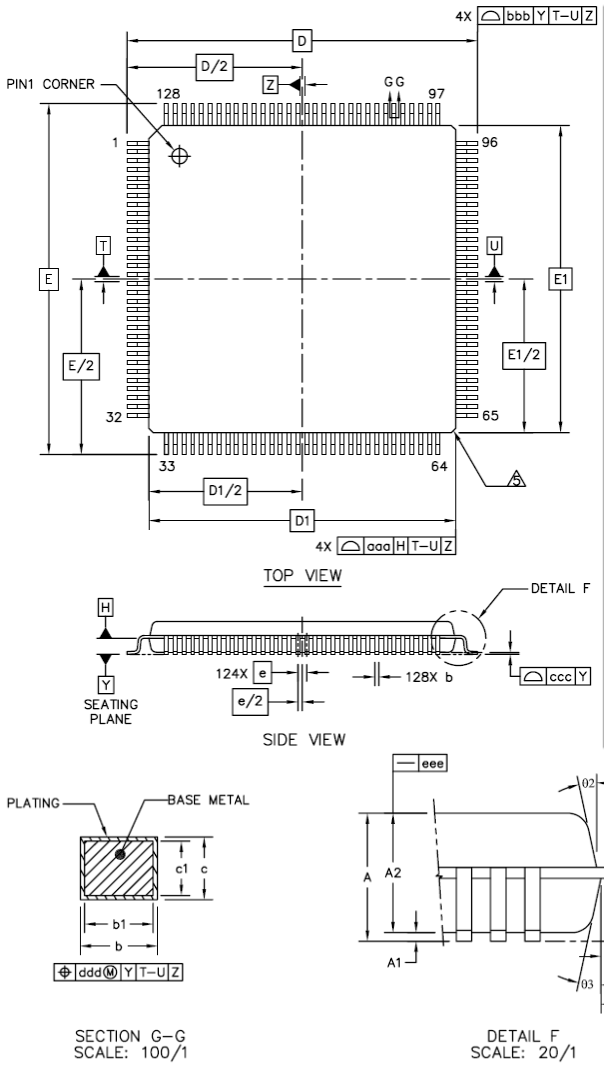
Version Identification:

Ex: For LAB version

The version shows on RED area. Ex: LXB

9. Package Dimensions (128-LQFP)

128 LQFP (14*14)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.16	0.23
LEAD WIDTH		b1	0.13	---	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	16 BSC		
	Y	E	16 BSC		
	X	D1	14 BSC		
	Y	E1	14 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

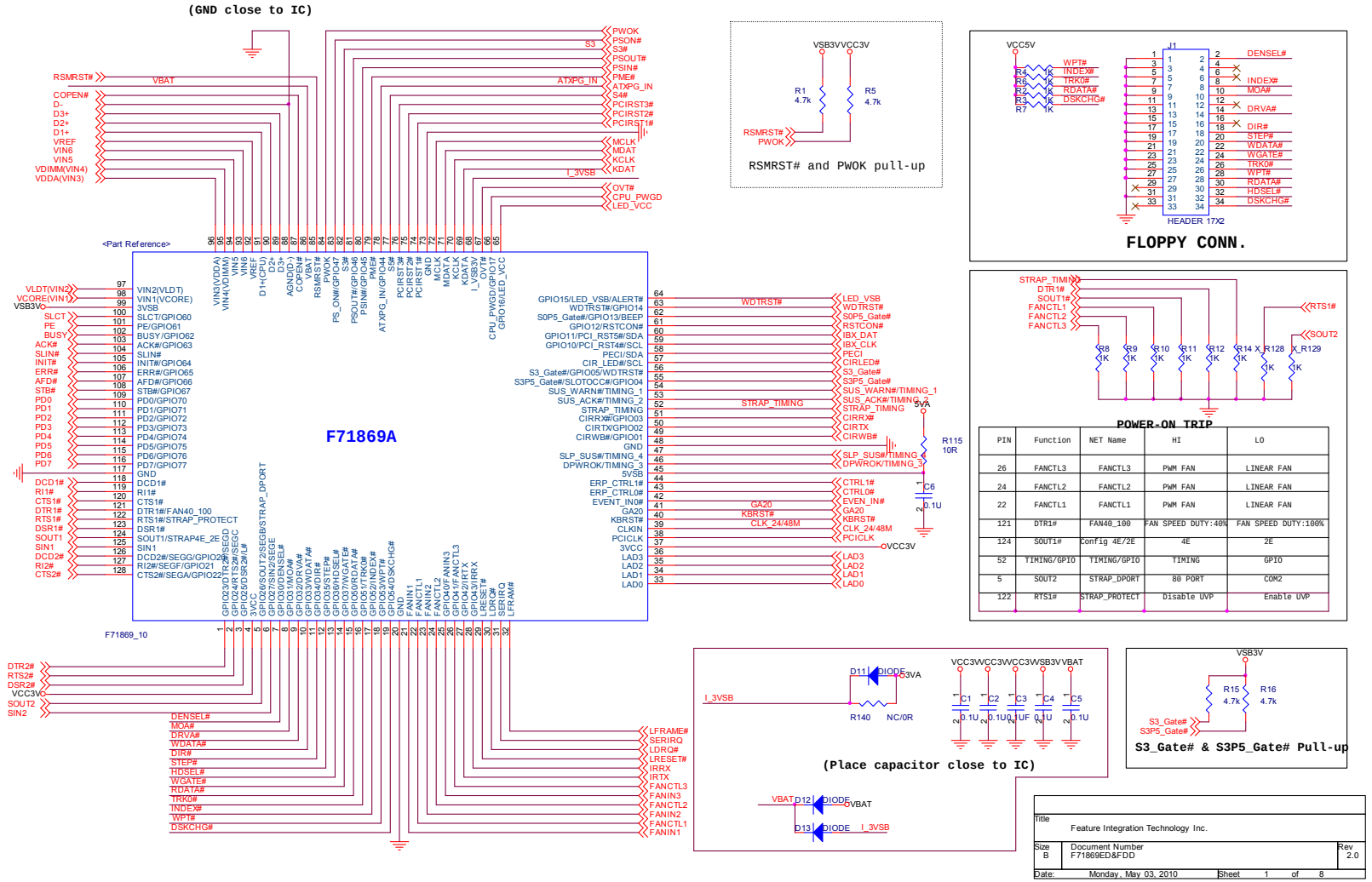
Feature Integration Technology Inc.

Headquarters
3F-7, No 36, Tai Yuan St.,
Chupei City, Hsinchu, Taiwan 302, R.O.C.
TEL : 886-3-5600168
FAX : 886-3-5600166
www: http://www.fintek.com.tw

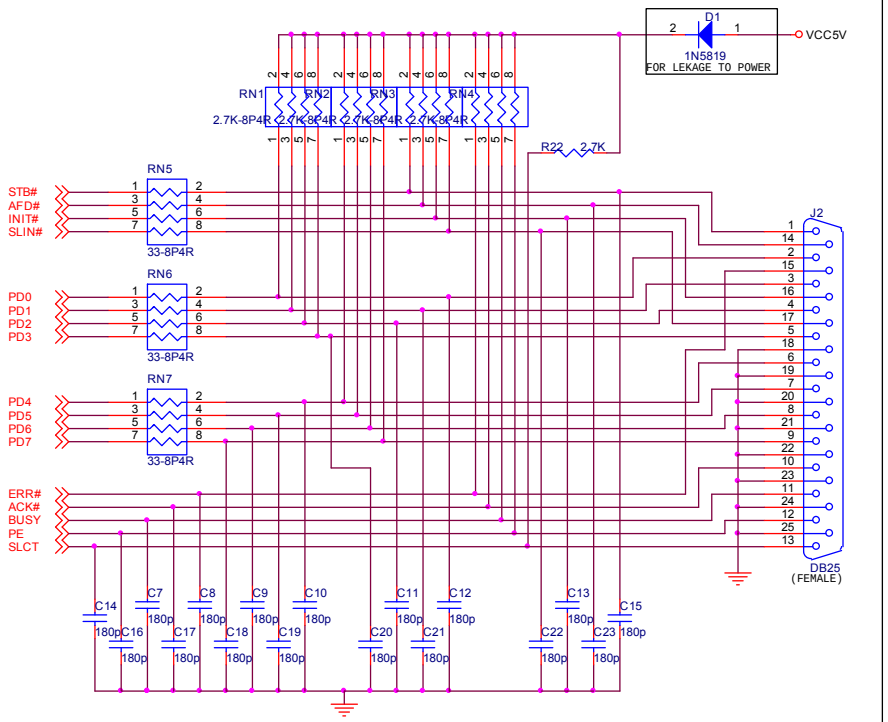
Taipei Office
Bldg. K4, 7F, No.700, Chung Cheng Rd.,
Chungho City, Taipei, Taiwan 235, R.O.C.
TEL : 866-2-8227-8027
FAX : 866-2-8227-8037

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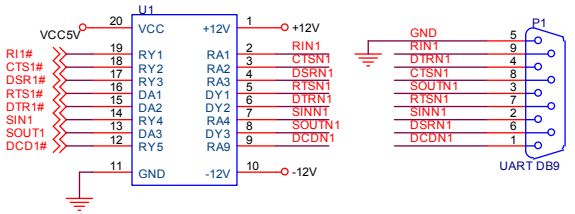
10. Application Circuit



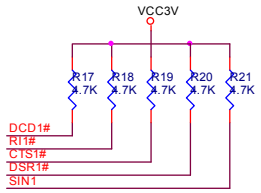
F71869A



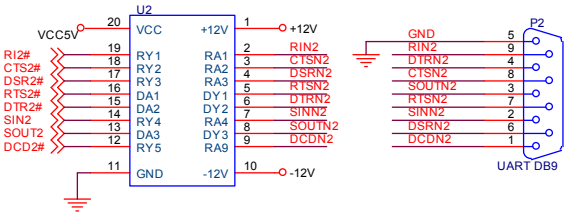
PARALLEL PORT INTERFACE



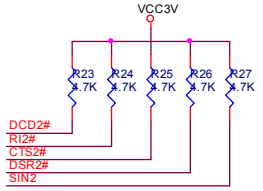
UART 1 PORT INTERFACE



If you do not use the UART port 1, please pull-up these pin to VCC3V.

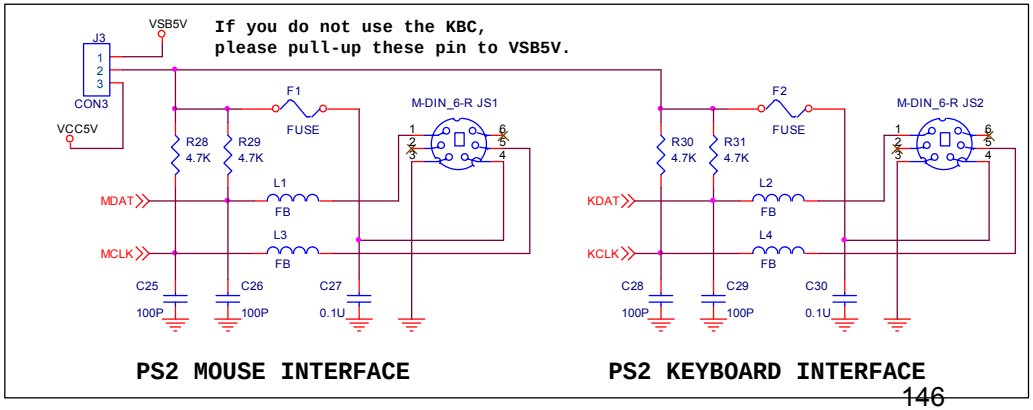


UART 2 PORT INTERFACE



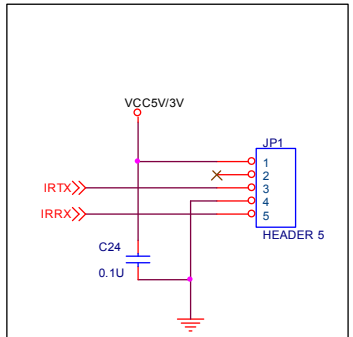
If you do not use the UART port 2, please pull-up these pin to VCC3V.

RING-IN Wake-up is supported by F71869E



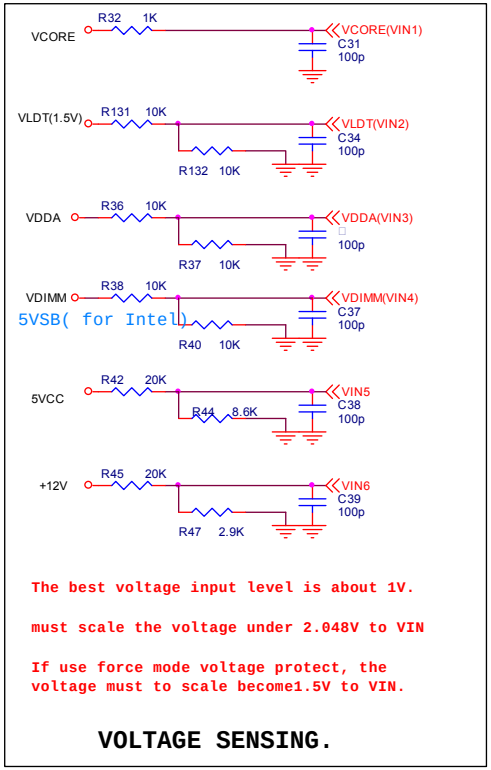
PS2 MOUSE INTERFACE

PS2 KEYBOARD INTERFACE

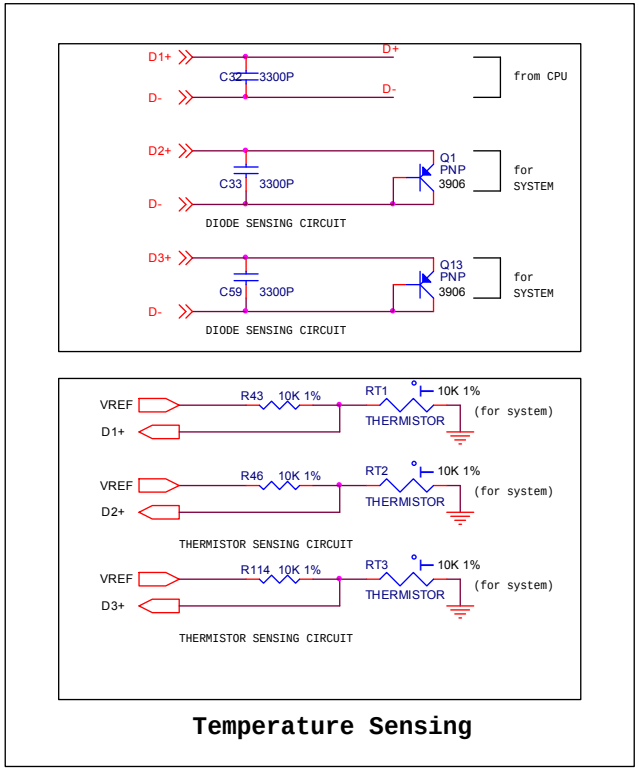


IR INTERFACE

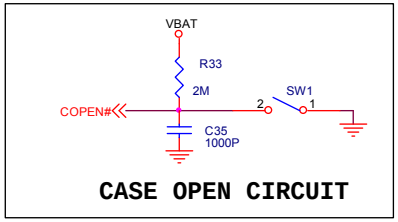
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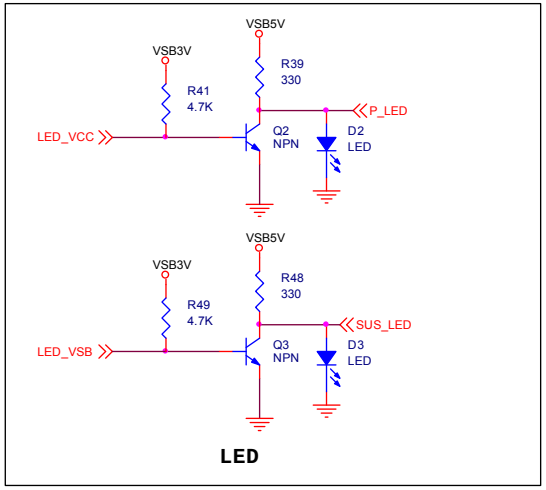
VOLTAGE SENSING.



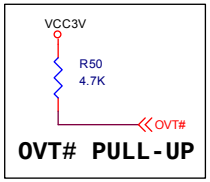
Temperature Sensing



CASE OPEN CIRCUIT

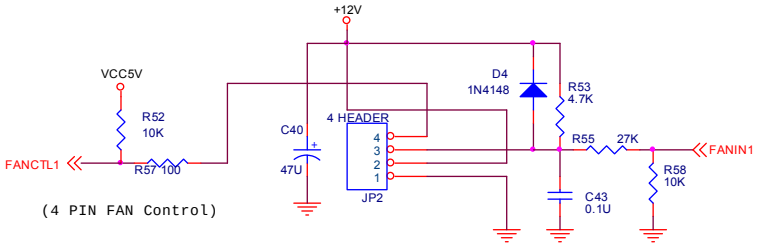


LED

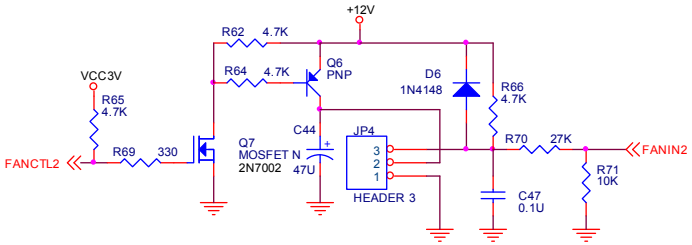


OVT# PULL-UP

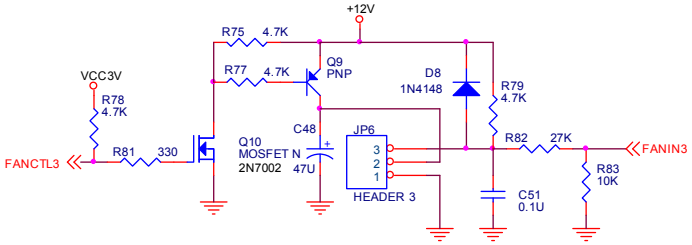
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Date: Friday, July 02, 2010	Sheet 8 of 8	July, 2010 V0.13P	



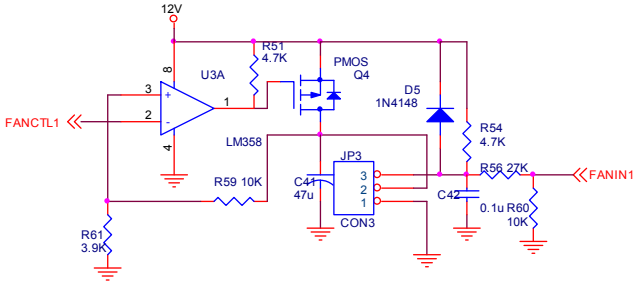
PWM FAN 1 SPEED CONTROL



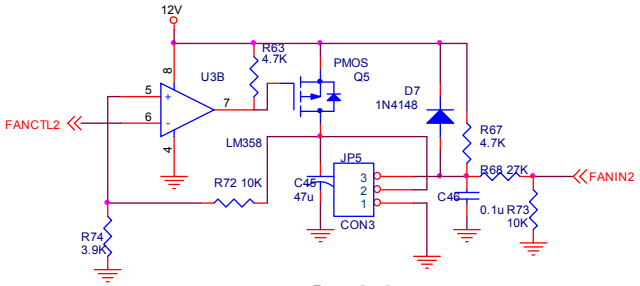
PWM FAN 2 SPEED CONTROL



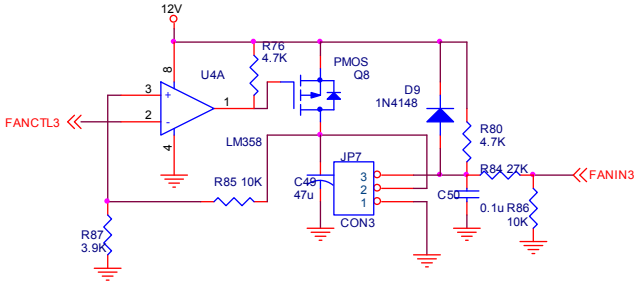
PWM FAN 3 SPEED CONTROL



DC FAN Control with OP 1



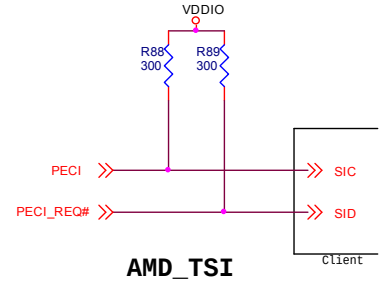
DC FAN Control with OP 2



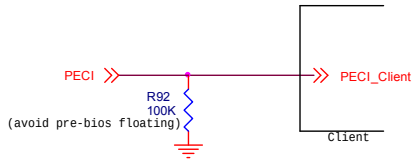
DC FAN Control with OP 3

FAN CONTROL FOR PWM OR DC

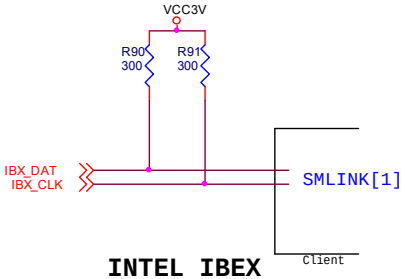
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Date: Friday, April 09, 2010	Sheet 4 of 8	



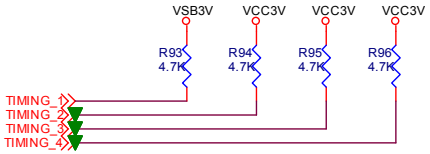
AMD_TSI



INTEL PECI



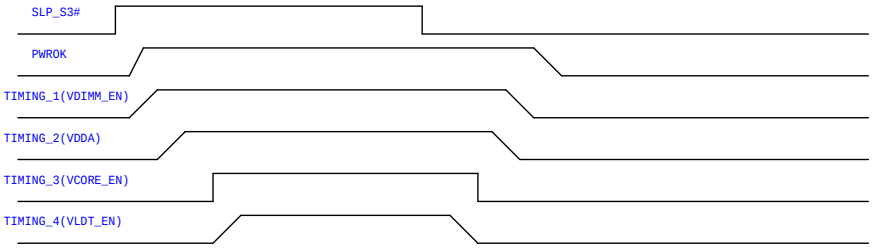
INTEL IBEX



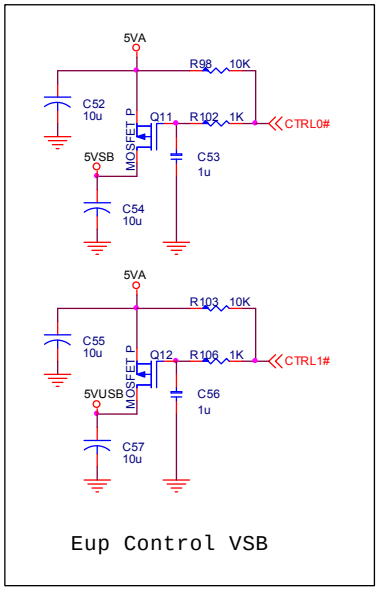
Power Sequence Pull-up

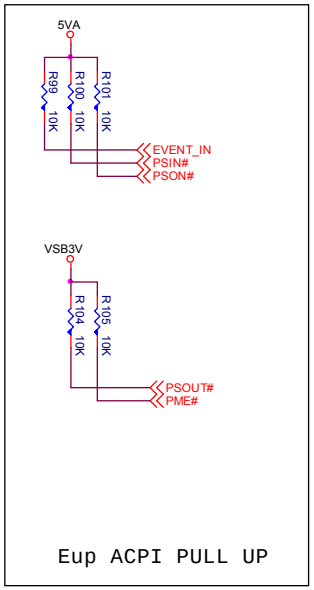


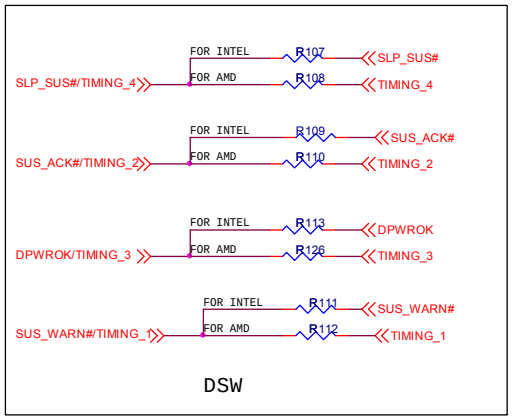
CPU_PWRGD Pull-Up

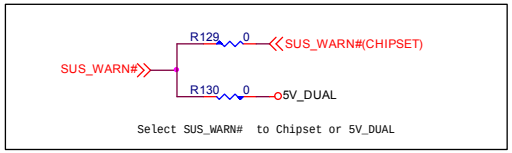


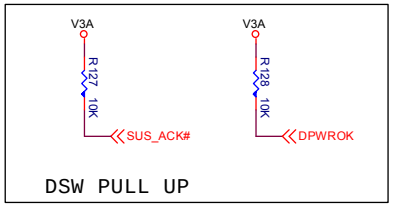
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Date: Monday, April 12, 2010	Sheet 8		



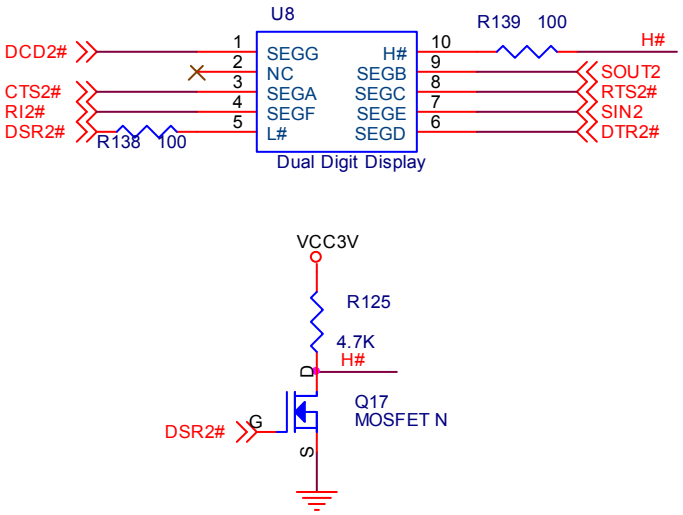






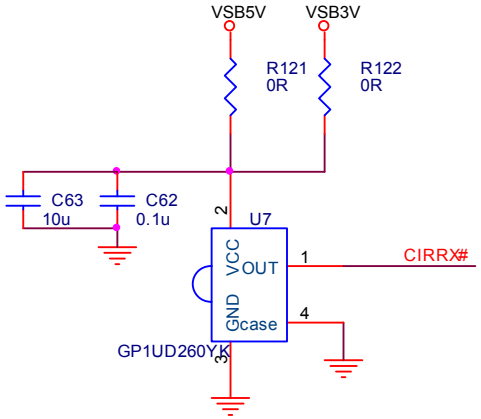


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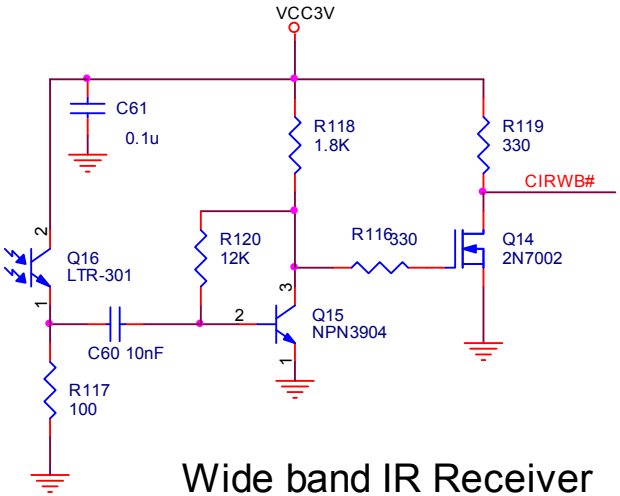
80 PORT 1 (output by COM2 interface)

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Size: A	Document Number: <Doc>		Rev: <Rev Code>
Date: Friday, April 09, 2010	Sheet 1 of 1		

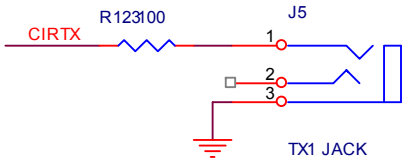


Long Rang IR Receiver

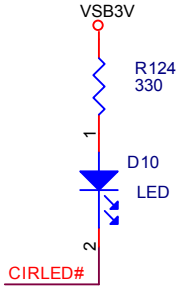
choose power and capacitance by IR receiver



Wide band IR Receiver



TX PORT



IR LED



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Date: Friday, April 09, 2010	Sheet 1 of 1	